Hall Ticket Number :										

R-19

Code: 19B41BT

M.Tech. I Semester Regular Examinations February 2020

Embedded System Concepts

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What is an embedded system? Describe the various hardware unit in embedded systems 6M

   b) What are the various software's used in an embedded system? 6M

OR

2. a) Demonstrate interrupt service routine with an example 6M

   b) What is meant by inter process communication? Explain in detail. 6M

UNIT–II

3. a) Summarize various structural units in a processor 6M

   b) How do you choose suitable processor for an embedded system? 6M

OR

4. Describe the working of DMA in detail. 12M

UNIT–III

5. a) What are the networks supported by the embedded systems? 6M

   b) Describe computer parallel communication using ISA and PCI 6M

OR

6. a) Explain RS232 bus communication interface in detail 6M

   b) Illustrate Round robin with interrupt with example 6M

UNIT–IV

7. a) Summarize the design methodologies in hardware-software co design 6M

   b) What are the various issues in system development process? 6M

OR

8. Illustrate the design cycle in the development face for an embedded system 12M

UNIT–V

9. Explain adaptive cruise car control with neat diagram 12M

OR

10. Explain the design of smart cards. 12M

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Hall Ticket Number :										

R-19

Code: 19B412T

M.Tech. I Semester Regular Examinations February 2020

Micro Computer System Design

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What are the advancements in 80286 processor when compared with 80186? 6M

   b) Explain the addressing modes for sequential control flow instructions with example. 6M

OR

2. a) Explain opcode prefetch queue in 8086? 6M

   b) Draw and discuss the structure of a general 80286 descriptor. 6M

UNIT–II

3. a) Explain the usage of the following registers of 80386.

      i) Segment Descriptor Registers.
      ii) Control Registers. 6M

   b) Explain the cache management unit of 80486. 6M

OR

4. a) Explain the different additional addressing modes supported by 80386? 6M

   b) Enlist the four major architectural advancements in 80486 over 80386. 6M

UNIT–III

5. a) Write short notes on the following:

      (i) Branch prediction.
      (ii) Out of order execution 6M

   b) Enlist the salient features of Pentium IV architecture. 6M

OR

6. a) Explain the Performance of Monitoring Registers of Pentium 4. 6M

   b) Write short note on dual core processors. 6M

UNIT–IV

7. a) Explain I/O design with suitable example. 6M

   b) How will you achieve a more sophisticated memory management scheme and explain with neat diagram. 6M

OR

8. Write short note on the following.

   i) Polling ii) daisy chain iii) Independent bus request scheme. 12M

UNIT–V

9. a) Discuss bit definitions of control word registers of 8087. 6M

   b) Write short note on MMX technology. 6M

OR

10. a) Discuss the register organizations of 8087. 6M

    b) Write short notes on SIMD technology. 6M

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Hall Ticket Number :										

R-19

Code: 19B411T

M.Tech. I Semester Regular Examinations February 2020

Modern Digital System Design

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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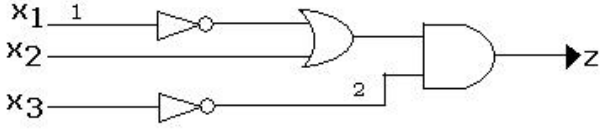
			Marks	CO	BL
		UNIT–I			
1.	a)	Explain the basic components of ASM chart.	4M	1	2
	b)	Develop the Implication matrix & Reduced state machine of the state table given below:			

Present State	Next State, Z			
	Inputs X_1 X_2			
	00	01	11	10
A	B, 0	D, 0	G, 1	A, 0
B	C, 1	G, 1	E, 0	B, 1
C	D, 1	G, 1	A, 0	C, 1
D	F, 1	H, 1	A, 0	D, 1
E	C, 0	F, 0	H, 1	E, 0
F	B, 1	H, 1	E, 0	F, 1
G	A, 0	E, 0	B, 1	D, 0
H	E, 0	A, 0	C, 1	F, 0

8M 1 3

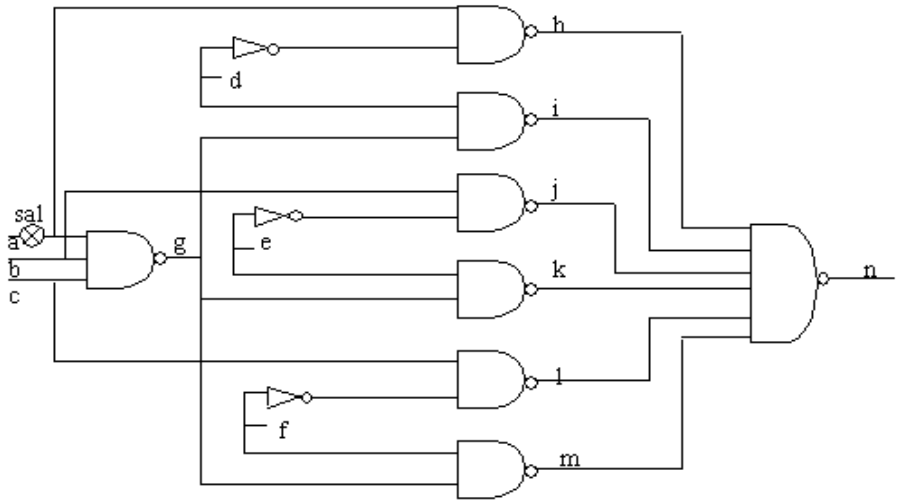
OR

2.	a)	Design a state machine to detect the overlapping sequence 1010 from the incoming bit stream and output '1' for each detection and implement it using PLA. Example: X: 10101010110- - - - - - - Z: 00010101000- - - - - - -	8M	1	3
	b)	Describe briefly about design of iterative circuits.	4M	1	2
		UNIT–I			
3.	a)	Using the path-sensitization method, find test vectors for SA-0 fault on input line 1 and SA-1 Fault on the internal line 2 of the circuit shown below: 	8M	2	3
	b)	Discuss briefly about the Signature analysis.	4M	2	2

OR

4. a) Discuss briefly about testing for bridging faults. 4M 2 2

   b) Generate the test vector to detect the S-A-1 fault at 'a' using D-Algorithm for the logic circuit given below:



8M 2 3

UNIT–III

5. Explain in detail the State identification and fault detection experiment in sequential circuits 12M 3 3

OR

6. a) Find the homing sequence for the state machine given below and write the output response table.

Present State	Next State, Z	
	X=0	X=1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

8M 3 3

   b) Write short notes on Synchronizing sequence. 4M 3 2

UNIT–IV

7. Find the Essential Prime Cubes of the following single output function using IISc algorithm, whenever necessary perform the sharp operations on the map.

   F= 1100 + 1211 + 0110 + 0001 + 2121 12M 4 3

OR

8. Describe the importance of PLA minimization and Folding in detail. 12M 4 3

UNIT–V

9. Discuss in detail the importance of Minimum closed cover in a fundamental mode model. 12M 5 3

OR

10. Explain in detail the Flow table and state reduction in a fundamental mode sequential circuit. 12M 5 3

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Hall Ticket Number :										

R-19

Code: 19BE11T

M.Tech. I Semester Regular Examinations February 2020

Research Methodology and IPR

(Common to All Branches)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. Explain the characteristics of a good research problem?

OR

2. Elucidate the different types of Data collection process.

UNIT–II

3. Explain the various types of research reports.

OR

4. Elucidate the format of writing a good research report.

UNIT–III

5. Elucidate the Patent Process.

OR

6. Explain the procedure for grants of Patents.

UNIT–IV

7. Elucidate the patent information and databases.

OR

8. Elucidate the scope of patent rights.

UNIT–V

9. Elucidate the IPR of Biological systems and Computer software.

OR

10. How to administrating patent system.

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Hall Ticket Number :										

R-19

Code: 19B41ET

M.Tech. I Semester Regular Examinations February 2020

System Modelling and Simulation

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. What is system simulation? Explain the steps involved in simulation study with Flowchart. 12M

OR

2. With suitable example explain discrete event Simulation 12M

UNIT–II

3. a) Compare the simulation packages with Programming Languages 6M

   b) Discuss the Software Features 6M

OR

4. Describe Object Oriented Simulation with suitable examples. How Object Oriented Simulation packages are differing from Application Oriented Simulation Packages 12M

UNIT–III

5. a) Discuss the Techniques for Increasing Model Validity and Credibility 6M

   b) How can you select input model without data? Explain with example 6M

OR

6. Define system integration. With neat sketches explain Motion Control models 12M

UNIT–IV

7. Write Short notes on
   (a) State Machines
   (b) System Encapsulation
   (c) Petri Nets. 12M

OR

8. Explain the Poisson Processes and Simulating a Poison Process 12M

UNIT–V

9. Describe the Simulating Queuing System and Types of Queues with an example. 12M

OR

10. Explain the Discrete-event System simulation and Steps in a Simulation Study 12M

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