Hall Ticket Number :										

R-14

Code: 4PB324

M.Tech. II Semester Regular & Supplementary Examinations June 2017

DSP Processors and Architectures

(Common to DECS, ES & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain the Digital Signal Processing system with the help of a block diagram. Also neatly sketch the typical signals in a DSP scheme. 5M

   b) Describe the basic feature that should be provided in the DSP architecture to be used to implement the Nth order FIR filter $y(n)=\sum_{i=0}^{N-1} h(i)x(n-i)$; n=0,1,2,… Where x(n) denotes the input sample ,y(n) the output sample and h(i) denotes the ith filter co-efficient. 7M

OR

2. a) Write and explain the fixed-point format for signals and co-efficient in DSP system. Find the range of numbers that can be represented in a fixed-point format using 16 bits if the number is treated as a signed integer and signed fraction. 5M

   b) Briefly explain the A/D conversion errors. 7M

UNIT–II

3. a) Implement a 3-bit shift right, barrel shifter. Tabulate the outputs fof different bit shifts. 8M

   b) Explain the different frequently used techniques to prevent overflow and underflow conditions occurring in MAC unit. 4M

OR

4. a) Explain with block diagram the implementation of 8 tap FIR filter,(i) pipelined using 8 MAC units and (ii) parallel using 2 MAC units. 8M

   b) Identify the Addressing modes of the operands in each of the following instructions and their operation. (i) ADD #1234h ,(ii) ADD B 4M

UNIT–III

5. a) Explain any three data addressing modes of TMS320C54xx. Give one example for each. 8M

   b) With a neat sketch, describe the Host port interface signal. 4M

OR

6. a) Assume that the contents of AR3 to be 400h, what will be its content after each of the following TMS320C54xx addressing mode is used. Assume that the contents of AR0=40h. (i) *AR3+ 0; (ii) *AR3+; (iii) *AR3 + 0B; 8M

   b) Describe the operation of the following instructions of TMS320C54XX processor. (i) MPY *AR2-,*AR4 + 0,B ; (ii) SSBX SXM ; (iii)RPT #k 4M

UNIT–IV

7. a) What values are represented by the 16 bit fixed point number N=2000h in the Q0,Q7 and Q15 notations. 8M

   b) Briefly explain the IIR filter. With the help of block diagram, explain second order IIR filter. 4M

OR

8. a) Explain how the bit-reversed index generation can be done in 8 point FFT. Also write a TMS320C54xx program for 8 point DIT FFT bit reversed index generation. 8M

   b) Explain, how scaling prevents overflow conditions in the butterfly computation. 4M

UNIT–V

9. a) What are interrupts? How interrupts are handled by the C54xx DSP processor. 8M

   b) Explain an interface between ban A/D converter and the TMS320C54xx processor in the programmed I/O mode. 4M

OR

10. a) Explain PCM3002 CODEC, with the help of a block diagram. 9M

    b) Draw the I/O interface timing diagram for the read-write-read sequence of operation. 3M

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Hall Ticket Number :										

R-14

Code: 4PB322

M.Tech. II Semester Regular & Supplementary Examinations June 2017

Embedded Software Design

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) What are the two versions available in Pentium? Compare and contrast Pentium with 80486 microprocessors. 6M

   b) Explain memory management unit in a Pentium processor 6M

OR

2. a) With neat diagram, explain a circuit that generates wait states by delaying ADS. 6M

   b) Explain super scalar architecture in a Pentium processor 6M

UNIT–II

3. a) Illustrate a laser printer design as an algorithm with neat sketch 6M

   b) Outline the checklist that can help you determine which RTOS products are suitable for your project 6M

OR

4. a) How the separation of hardware and software design imposes development costs 6M

   b) From the perspective of hardware designer and software designer, explain how to solve the Big Endian / Little Endian Problem. 6M

UNIT–III

5. a) Outline a memory map of a generic microprocessor with how the system uses memory with the execution environment for a new system. 6M

   b) What is an ISR? Give the flow chart for a Burglar alarm algorithm 6M

OR

6. a) What is watchdog timer? Give the flow diagram. 6M

   b) List the advantages and disadvantages of the debug kernel 6M

UNIT–IV

7. a) What is JTAG? Give a simple schematic representation of a JTAG loop for three circuit elements. 6M

   b) What is Overlay Memory? Explain. 6M

OR

8. a) Explain the advantages and disadvantages of back ground debug mode 6M

   b) Discuss about White box, Black box and Gray box Testing. 6M

UNIT–V

9. a) Discuss various methods used to dump the code in to target system 6M

   b) Discuss various kinds of buffers & explain the reasons for occurring over and under –run states 6M

OR

10. a) Explain the importance of Emulation and Debugging techniques in embedded system 6M

    b) What are buffers? Explain linear buffers and direction buffers. 6M

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Hall Ticket Number :										

Code: 4PB323

R-14

M.Tech. II Semester Regular & Supplementary Examinations June 2017

Hardware Software Co-Design

(Common to ES & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. Construct a FSMD model for capturing the behavior of Co-synthesis system using an example 12M

OR

2. a) State and explain various Co-design languages. 6M
   b) Describe the distributed system Co-Synthesis. 6M

UNIT–II

3. Elucidate what is system specialization and explain its techniques in detail 12M

OR

4. a) Write short notes on shared memory communication scheme 6M
   b) Describe an architecture that can be used in data dominated applications 6M

UNIT–III

5. What is meant by compilation? Discuss practical considerations in a Compiler Development Environment for embedded systems 12M

OR

6. a) With the help of block diagram explain modern Embedded Architecture. 6M
   b) Elucidate the concept of retargetable compiler 6M

UNIT–IV

7. With a suitable example explain the methodology involved in the Co-design Computational model. 12M

OR

8. a) Classify coordinating concurrent computation mechanisms 6M
   b) Write short notes on Interfacing Components. 6M

UNIT–V

9. Summarize various types of system level specification schemes and discuss about them briefly 12M

OR

10. a) Elaborate briefly about various Multi language validation approaches. 6M
    b) List characteristics of Lycos system 6M

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Hall Ticket Number :										

Code: 4PB325

R-14

M.Tech. II Semester Regular & Supplementary Examinations June 2017

Modelling and Synthesis through Verilog HDL

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Discuss about Verilog Primitives used in Hardware Modeling and write briefly about various descriptive Styles. 6M
   b) Write Verilog code for a Half Adder using built-in primitives. 6M

OR

2. a) Outline the various Constants and Operators used in Verilog. 6M
   b) Write brief notes on language conventions in Verilog. 6M

UNIT–II

3. a) Explain briefly about the Propagation Delay using built-in constructs. 6M
   b) Discuss briefly the importance of Time Scales used for Simulation in Verilog. 6M

OR

4. a) Illustrate the initialization of sequential primitives with relevant examples. 6M
   b) Explain briefly the importance of Pulse rejection? 6M

UNIT–III

5. a) Implement NAND gate using MOS switch and write a suitable test bench? 6M
   b) Summarize about the delay constructs in Verilog. 6M

OR

6. a) What is Procedural Assignment? Write a sample program using Procedural Continuous Assignments. 6M
   b) Explain the fork & join statements and when they are used. 6M

UNIT–IV

7. Explain the importance of the Don't cares, Tri-State outputs and the Tri-state Buffers? 12M

OR

8. a) Explain the Synthesis of Edge-Triggered D-Flip Flop. 6M
   b) Illustrate the synthesis of a basic Finite State Machines in verilog. 6M

UNIT–V

9. a) Discuss about the restrictions imposed on Synthesis of 'Z' and 'X'. 6M
   b) Explain briefly about the synthesis of Multi-cycle operations? 6M

OR

10. Discuss the Synthesis of Case and Conditional Statement. Explain them with suitable examples. 12M

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Hall Ticket Number :										

R-14

Code: 4PB326

M.Tech. II Semester Regular & Supplementary Examinations June 2017

Radio Frequency Identification

(Embedded Systems)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain optical Character Recognition system. 6M
   b) Explain the process of Information processing in the Transponder. 6M

OR

2. a) Distinguish the various Identification Systems with system Parameters 6M
   b) Explain the selection criteria for RFID systems 6M

UNIT–II

3. a) Explain Electromagnetic Backscatter coupling 6M
   b Define and explain Active and Passive modes of Near Field Communication (NFC) 6M

OR

4. Explain the selection of a suitable frequency for Inductively coupled RFID system with suitable example. 12M

UNIT–III

5. a) Explain the significance of Transponder with memory function 6M
   b) Explain Dual Interface card. 6M

OR

6. a) Explain the Transponder with sensor function measurements. 6M
   b) Draw and Explain Frequency Shift Keying Modulation procedure. 6M

UNIT–IV

7. a) Explain LRC and CRC Procedures 6M
   b) Explain RF Interface Protection by Cryptographic Measures 6M

OR

8. Draw and Explain the Anti-collision procedures through FDMA and TDMA. 12M

UNIT–V

9 Explain on the following RFID Applications:
   (i) Contactless Smart Cards 6M
   (ii) Electronic Passport Transport Systems 6M

OR

10. Explain any Two NFC applications of RFID systems. 12M

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Hall Ticket Number :										

R-14

Code: 4PB321

M.Tech. II Semester Regular & Supplementary Examinations June 2017

Testing and Testability

(Common to ES & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. Describe Gate level and Event driven simulation. 12M

OR

2. Classify Modeling of digital circuits and explain. 12M

UNIT–II

3. Explain in detail about single stuck-at and multiple stuck-at faults with an example of each. 12M

OR

4. Write short notes on the following
   (a) Fault detection and Redundancy. 6M
   (b) Fault equivalence and fault location. 6M

UNIT–III

5. Explain Test pattern generation, Syndrome test and Signature analysis. 12M

OR

6. Discuss different compression techniques. 12M

UNIT–IV

7. Describe board level and system level DFT approaches. 12M

OR

8. Explain the following
   (a) Controllability and Absorbability 6M
   (b) Boundary scan standards 6M

UNIT–V

9. Discuss BIST concepts, JTAG testing 12M

OR

10. Discuss about Advanced BIST concepts, specific BIST architectures. 12M

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