Hall Ticket Number :										

R-14

Code: 4PC322

M.Tech. II Semester Regular & Supplementary Examinations June 2017

ASIC Design

(V L S I System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Write in detail about Full - Custom & Semi – Custom ASICs. 6M
   b) Define Gate – Masked Gate Array (MGA) and Explain their types in detail. 6M

OR

2. a) Describe in detail about ASIC Design Flow with neat sketches. 6M
   b) List and Compare different ASIC Technologies. 6M

UNIT–II

3. a) Draw the structure of ASIC Programmable Logic Device and Explain. 8M
   b) Write short notes on features of Programmable Logic Devices. 4M

OR

4. a) Explain about Design methodologies of ASICs. 6M
   b) Compare different ASIC Technologies and explain. 6M

UNIT–III

5. a) Describe different performance characteristics of ASICs. 6M
   b) Draw and explain the operation of standard cells used in ASIC Design. 6M

OR

6. a) Explain in detail about ASIC Design styles. 8M
   b) Write short notes on ASIC cell libraries. 4M

UNIT–IV

7. a) With neat sketch explain in detail about HDL based design flow. 6M
   b) Explain commercially available tools for ASIC Design. 6M

OR

8. a) Define synthesis and explain in detail. 6M
   b) Explain simulation mechanisms used for ASIC design. 6M

UNIT–V

9. a) Explain in detail about floor planning in ASIC Design. 6M
   b) Explain the following
      i. Clock distribution
      ii. Timing-Driven Place/Route 6M

OR

10. a) Write in detail about routing mechanisms in FPGA. 8M
    b) Write short on Design Rule Check (DRC) for ASICs. 4M

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M.Tech. II Semester Regular & Supplementary Examinations June 2017

Algorithms for VLSI Design Automation

(V L S I System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain the principle of Dijkstra's Shortest-path Algorithm.
   b) With an example elaborate the combinatorial optimization problem.

OR

2. a) Describe the methods of computation of the shortest path in a graph.
   b) How ILP can be used to optimize the TSP?

UNIT–II

3. a) What is compiler-driven simulation?
   b) Elaborate the concept of connectivity and signal modelling.

OR

4. a) Highlights on the general remarks of VLSI simulation.
   b) Write the concept of simulation mechanisms.

UNIT–III

5. a) What are the basic issues in combinational logic synthesis?
   b) Writ the VHDL code for a 4-bit universal counter.

OR

6. a) What is two-level logic synthesis?
   b) Justify the need for ROBDD manipulation.

UNIT–IV

7. a) How does mobility-based scheduling works?
   b) What is clique partitioning?

OR

8. a) Elucidate the concept of force-directed scheduling.
   b) With an example elaborate the iterative data flow method.

UNIT–V

9. Explain the concept of the routing algorithms for the segmented model.

OR

10. a) Write short notes on: FPGA Technologies
    b) Topological routing

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Hall Ticket Number :										

R-14

Code: 4PB324

M.Tech. II Semester Regular & Supplementary Examinations June 2017

DSP Processors and Architectures

(Common to DECS, ES & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain the Digital Signal Processing system with the help of a block diagram. Also neatly sketch the typical signals in a DSP scheme. 5M

   b) Describe the basic feature that should be provided in the DSP architecture to be used to implement the Nth order FIR filter $y(n)=\sum_{i=0}^{N-1} h(i)x(n-i)$; n=0,1,2,… Where x(n) denotes the input sample ,y(n) the output sample and h(i) denotes the ith filter co-efficient. 7M

OR

2. a) Write and explain the fixed-point format for signals and co-efficient in DSP system. Find the range of numbers that can be represented in a fixed-point format using 16 bits if the number is treated as a signed integer and signed fraction. 5M

   b) Briefly explain the A/D conversion errors. 7M

UNIT–II

3. a) Implement a 3-bit shift right, barrel shifter. Tabulate the outputs fof different bit shifts. 8M

   b) Explain the different frequently used techniques to prevent overflow and underflow conditions occurring in MAC unit. 4M

OR

4. a) Explain with block diagram the implementation of 8 tap FIR filter,(i) pipelined using 8 MAC units and (ii) parallel using 2 MAC units. 8M

   b) Identify the Addressing modes of the operands in each of the following instructions and their operation. (i) ADD #1234h ,(ii) ADD B 4M

UNIT–III

5. a) Explain any three data addressing modes of TMS320C54xx. Give one example for each. 8M

   b) With a neat sketch, describe the Host port interface signal. 4M

OR

6. a) Assume that the contents of AR3 to be 400h, what will be its content after each of the following TMS320C54xx addressing mode is used. Assume that the contents of AR0=40h. (i) *AR3+ 0; (ii) *AR3+; (iii) *AR3 + 0B; 8M

   b) Describe the operation of the following instructions of TMS320C54XX processor. (i) MPY *AR2-,*AR4 + 0,B ; (ii) SSBX SXM ; (iii)RPT #k 4M

UNIT–IV

7. a) What values are represented by the 16 bit fixed point number N=2000h in the Q0,Q7 and Q15 notations. 8M

   b) Briefly explain the IIR filter. With the help of block diagram, explain second order IIR filter. 4M

OR

8. a) Explain how the bit-reversed index generation can be done in 8 point FFT. Also write a TMS320C54xx program for 8 point DIT FFT bit reversed index generation. 8M

   b) Explain, how scaling prevents overflow conditions in the butterfly computation. 4M

UNIT–V

9. a) What are interrupts? How interrupts are handled by the C54xx DSP processor. 8M

   b) Explain an interface between ban A/D converter and the TMS320C54xx processor in the programmed I/O mode. 4M

OR

10. a) Explain PCM3002 CODEC, with the help of a block diagram. 9M

    b) Draw the I/O interface timing diagram for the read-write-read sequence of operation. 3M

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M.Tech. II Semester Regular & Supplementary Examinations June 2017

Hardware Software Co-Design

(Common to ES & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. Construct a FSMD model for capturing the behavior of Co-synthesis system using an example 12M

OR

2. a) State and explain various Co-design languages. 6M
   b) Describe the distributed system Co-Synthesis. 6M

UNIT–II

3. Elucidate what is system specialization and explain its techniques in detail 12M

OR

4. a) Write short notes on shared memory communication scheme 6M
   b) Describe an architecture that can be used in data dominated applications 6M

UNIT–III

5. What is meant by compilation? Discuss practical considerations in a Compiler Development Environment for embedded systems 12M

OR

6. a) With the help of block diagram explain modern Embedded Architecture. 6M
   b) Elucidate the concept of retargetable compiler 6M

UNIT–IV

7. With a suitable example explain the methodology involved in the Co-design Computational model. 12M

OR

8. a) Classify coordinating concurrent computation mechanisms 6M
   b) Write short notes on Interfacing Components. 6M

UNIT–V

9. Summarize various types of system level specification schemes and discuss about them briefly 12M

OR

10. a) Elaborate briefly about various Multi language validation approaches. 6M
    b) List characteristics of Lycos system 6M

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Code: 4PC321

M.Tech. II Semester Regular & Supplementary Examinations June 2017

Low Power VLSI Design

(VLSI System Design)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. a) Explain the following low-voltage, low-power design limitations
   (i) power supply voltage
   (ii) Threshold voltage 6M

   b) Explain Deep Trench isolation technique 6M

OR

2. a) How threshold voltage adjustments can be carried out for CMOS devices? Explain with the help of necessary equations. 6M

   b) Explain Retrograde-well CMOS process. 6M

UNIT–II

3. Explain the low voltage / low power lateral BJT on SOI process. 12M

OR

4. Explain the following future trends and directions of CMOS/BiCMOS processes.
   (i) Technology
   (ii) Bipolar device structure improvements 12M

UNIT–III

5. a) Describe level 1 and level 2 models of MOSFET 6M

   b) Describe the sub threshold current model of MOSFET with necessary equations,. 6M

OR

6. Explain the following Bipolar models
   (i) Ebers-Moll model
   (ii) Gummel- Poon model 12M

UNIT–IV

7. Explain briefly about BiCMOS circuits utilizing Lateral pnp BJTs in PMOS structures. 12M

OR

8. Explain ESD-free Bi-CMOS digital circuit operation and comparative analysis. 12M

UNIT–V

9. a) Explain the functionality theme and synchronous themes of latches and flip-flops. 6M

   b) What are the performance measures of latches and flip-flops? 6M

OR

10. Explain briefly about power reduction in clock networks. 12M

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Code: 4PB321

M.Tech. II Semester Regular & Supplementary Examinations June 2017

Testing and Testability

(Common to ES & VLSISD)

Max. Marks: 60 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 12 = 60 Marks)

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UNIT–I

1. Describe Gate level and Event driven simulation. 12M

OR

2. Classify Modeling of digital circuits and explain. 12M

UNIT–II

3. Explain in detail about single stuck-at and multiple stuck-at faults with an example of each. 12M

OR

4. Write short notes on the following
   (a) Fault detection and Redundancy. 6M
   (b) Fault equivalence and fault location. 6M

UNIT–III

5. Explain Test pattern generation, Syndrome test and Signature analysis. 12M

OR

6. Discuss different compression techniques. 12M

UNIT–IV

7. Describe board level and system level DFT approaches. 12M

OR

8. Explain the following
   (a) Controllability and Absorbability 6M
   (b) Boundary scan standards 6M

UNIT–V

9. Discuss BIST concepts, JTAG testing 12M

OR

10. Discuss about Advanced BIST concepts, specific BIST architectures. 12M

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