Code : 1PA312

R-11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I Semester Regular/Supplementary Examinations April - 2013

Advanced Digital Signal Processing
(DECS)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a) Define and classify Discrete time systems. Check whether the following is a Linear system or not. $Y[n]=5x[n]+2x[n]^2$ 6M

   b) Find the DTFT and also draw magnitude and phase response of the following sequence $x[n]=\{1,1,2,2,3,3,4,4\}$ 6M

2. a) Explain the method of designing IIR Filters using Pade approximation Method. 6M

   b) Explain about Poly phase realization of FIR filters. 6M

3 a) Explain about Chirp Z transform for the calculation of DFT of a sequence. 6M

   b) Explain Index mapping method of computation of DFT. 6M

4 a) Derive the Frequency domain response expression for Decimator. 6M

   b) Explain with an example procedure for the implementation of sampling rate conversion with cascaded integrator comb filters. 6M

5 a) Explain Burg method of Power Spectrum estimation. 6M

   b) Explain Levison-Durbin Algorithm. 6M

6 a) Write Notes on

   i) Daubechies Wavelet

   ii) Short Time Fourier Transform. 6M

   b) What is Filter Bank? Explain how DFT acts as a Filter Bank. 6M

7 a) Explain about multilevel decomposition in Wavelet Transforms. 6M

   b) What is the difference between continuous wavelet and Discrete wavelet transforms. Explain. 6M

8 Write short notes on

   a) Spectral Analysis of Non stationary signals. 6M

   b) Oversampling A/D converters. 6M

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M.Tech. I Semester Regular/Supplementary Examinations April - 2013

Digital Communication Techniques
(DECS)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1.		What is the probability density function? Obtain Gaussian, Rayleigh and Rayleigh Probability Density Functions.	12M
2.	a)	Explain Signal Space Concepts.	6M
	b)	Briefly explain a Signal Space Concepts.	6M
3.		Explain different digital modulation technique.	12M
4.		How AWGN channel can be optimized by its receiver and obtain waveform for AWGN channel.	12M
5.	a)	Explain Statistical Models for fading channels.	6M
	b)	Explain Diversity Techniques for fading Multipath Channels.	6M
6.	a)	Explain the generalized RAKE demodulator.	6M
	b)	Explain a tapped delay line channel modulator.	6M
7.	a)	Prove the effect ISI using necessary block diagram.	6M
	b)	Explain different equalization technique.	6M
8.		What is the necessary of OFDM and Explain Filter bank implementation of OFDM Receiver.	12M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I Semester Regular/Supplementary Examinations April - 2013

Digital System Design
(DECS)
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Max. Marks: 60 **Time: 03 Hours**

Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a) Discuss in detail about reduction of state tables and state assignments 6M
   b) Draw an ASM chart of JK flip flop. Realize it using SR flip flop and required gates 6M
2. a) Draw the general structure of a CPLD and explain how a logic function can be realized on CPLD with simple example 6M
   b) Design and implement a BCD counter on PLD (PLA). Draw the complete fuse-map circuit 6M
3. a) What are the different faults found in combinational circuits? How can they be categorized? 6M
   b) Draw the circuit which realizes the function f(x) = x1 x2 + x3 x4 using AND-OR gates using Boolean difference method, obtain the test set to detect SAo fault on input line x1 of the circuit. 6M
4. a) Explain the procedure to find SA0 & SA1 fault for Non Redundant Circuits using D-Algorithm with suitable example? 8M
   b) With an example, explain the transition count testing method. 4M
5. a) Write note on different state identification experiments with one example each 6M
   b) Find a preset distinguishing experiment that determines the initial state of the machine shown in table given below. Given that it cannot be initially in state E. 6M

Ps	Ns, z x=0 , x=1
A	B,1 A,1
B	E,0 A,1
C	A,0 E,1
D	C,1 D,1
E	E,0 D,1

6. a) Briefly describe about PLA folding. 6M
   b) Design a 3 bit BCD to grey code converter and realize the circuit using PLA and then show that how folding will reduce the number of cross points given on the PLA. 6M
7. a) List out and explain briefly about the faults that may occur in PLAs 6M
   b) With an example, explain how faults are detected in a PLA. 6M
8. a) Define the races and cycles in sequential circuits. 8M
   b) Write note on Minimal Closed Covers 4M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I Semester Regular/Supplementary Examinations April - 2013

Embedded System Concepts
(DECS, ES and VLSI SD)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1.	a)	Explain the softwares in designing an Embedded system	8M
	b)	What is the importance of device drivers?	4M
2.	a)	Explain different interfacing devices to connect memories and devices in an Embedded system	8M
	b)	Write short notes on memory allocation.	4M
3.	a)	Differentiate OS and RTOS.	4M
	b)	Explain function queue scheduling.	8M
4.		Discuss the problems in sharing the data in multitask environment. How to overcome the problems	12M
5.		Explain the system analysis and system design procedure for designing an embedded system	12M
6.		Give the specification details in designing Embedded system.	12M
7.		Write short notes on ICE and IDE.	12M
8.		Design and develop an Embedded system for digital camera.	12M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I Semester Regular/Supplementary Examinations April – 2013

Hardware Description Languages
(DECS and VLSI SD)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1.	a)	Discuss about Structural, Behavioral and Hierarchical design descriptions in Verilog?	8M
	b)	Write about Language conventions?	4M
2.	a)	Explain the need for Simulation. Discuss analog and discrete event simulations?	8M
	b)	What are the Delay models available in Verilog?	4M
3.	a)	Explain Procedural timing control and synchronization with examples?	8M
	b)	Compare Static and Dynamic timing analysis?	4M
4.		What are the general rules for Combinational synthesis?. Explain in terms of net-list of primitives, UDPs, Cyclic behavior and Function/Tasks?	12M
5.		Explain Synthesis of Structured ICs in Verilog?	12M
6.		Explain Switch-level models in Verilog?	12M
7.	a)	Explain about design Verification tools for VHDL?	8M
	b)	Explain delay model and simulation in VHDL?	4M
8.		Write Short notes, answer any three a. Basic Chip design flow b. System tasks, Functions and Syntax c. DFT in VHDL d. VHDL coding styles	4x3=12M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I Semester Regular/Supplementary Examinations April - 2013

Wireless Communications
(DECS)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. Discuss blue tooth, WLL & Personal Area Network with an example.
2. a) Discuss Two Ray ground reflection model.
   b) Discuss the factors in the radio propagation channel that influence the small scale fading.
3. a) Determine the distribution of Rayleigh fading ($\gamma\sum$) by differentiating $P\gamma\sum(\gamma)$ relative to γ, and we obtain the outage probability by evaluating $P\gamma\sum(\gamma)$ at $\gamma = \gamma 0$.
   b) What is diversity? Derive expression for maximal ratio.
4. What are the different types multiple access techniques used for sharing the available bandwidth in the wireless communication system? Brief out any one technique.
5. a) Discuss briefly about direct sequence spread spectrum with neat sketch.
   b) Discuss briefly about
   a) Time hopping b) Anti jamming..
6. Draw and explain the modulator and demodulator of Multiple carrier CDMA system.
7. What is MIMO system? Explain in detail about Narrow band multiple antenna system model?
8. Discuss the GSM specifications and air interface of 3G wireless network.

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