Code : 1PC314

R11

M.Tech. I Semester Supplementary Examinations, July/August 2014

Hardware Description Languages

(Common to DECS & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1. a) Write the differences between Structural and Behavioral Description In Verilog with an example. 6M

   b) Write about Data Types, Strings, Constants, and Operators in HDL. 6M

2. a) Design half-adder module with time delay assignment through parameter declaration. 6M

   b) Give the test bench, simulation results for the above module. 6M

3. a) What are the various delay constructs in Verilog? 4M

   b) Write syntax for Behavioral Statements, Procedural Assignment, and Procedural Continuous Assignments by taking a simple example. 8M

4. a) What is the difference between combinational and sequential logic circuits? Explain with examples. 6M

   b) Explain how to synthesize Latches, Edge-Triggered Flip Flops, Finite State Machines 6M

5. a) What is meant by synthesis of a design? How it is useful in hardware design? 6M

   b) Write about synthesis of language constructs Nets, Register Variables, Expressions and Operators. 6M

6. a) Write the differences between pass transistor logic and transmission gate logic. Draw transmission gate and write the Verilog code for it. 6M

   b) Write about Signal Strengths and Wired Logic in Switch-level models. 6M

7. a) What is VHDL? Give the importance. Write Some of the CAD tools used in VLSI. 4M

   b) Explain the terms Simulation, Optimization, Place and Route in VHDL. 8M

8. a) Write the differences between VHDL and Verilog. 5M

   b) Write VHDL code for full-adder circuit using Assertion Statements 7M

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Code : 1PA312

R11

M.Tech. I Semester Supplementary Examinations, July/August 2014

Advanced Digital Signal Processing

(DECS)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Determine the zero – input – response of the system described by second order difference equation $y(n) = \frac{5}{6}y(n-1) - \frac{1}{6}y(n-2) + x(n)$ 6M

   b) Discuss the properties of Discrete Time Fourier Transform. 6M

2. a) What are different linear phase transfer functions? 6M

   b) Explain the design of computationally efficient FIR filters. 6M

3. a) Draw the block diagram to illustrate the implementation of chirp – Z Transform for computing the DFT & explain. 6M

   b) Explain about split Radix FFT. 6M

4. a) Explain the decimation process with an example. 6M

   b) Why multirate sampling is required and where it is used? 6M

5. a) Compare parametric and non-parametric power spectrum estimation methods. 6M

   b) Explain the MA, ARMA models. 6M

6. a) Explain the application of Wavelets in signal compression. 6M

   b) What is Filter-Bank? Discuss about Uniform DFT filter bank. 6M

7. a) Explain reconstruction filter with reconstructing approximations. 6M

   b) What is wavelet packet synthesis and explain in detail. 6M

8. a) Explain how digital signal processing is applicable for musical sound processing? 6M

   b) Explain about discrete – time analytic signal generation. 6M

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Code : 1PB311

R11

M.Tech. I Semester Supplementary Examinations, July/August 2014

EMBEDDED SYSTEM CONCEPTS

(Common to DECS, ES and VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1. Explain Embedded System-On-Chip (SOC) and its components in detail.

2. Explain how separate caches for instruction, data and branch transfer help in speed up of a system.

3. Explain how asynchronous, synchronous and iso-synchronous communication devices are handled in embedded systems? Write note on RS232C/RS485 communication standards?

4. Write note on possible problems faced, while sharing data by multiple tasks and routines and give their solutions.

5. Describe different system design methodologies? Explain how requirement analysis is done.

6. Write a detail note on embedded software development process and tools?

7. Write note on hardware laboratory tools used in prototype development and testing of embedded system design?

8. Describe a design example for adaptive cruise control in a car?

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