Code : *1PC314*

R-11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I- Semester *Supplementary Examinations, November 2012*

HARDWARE DESCRIPTION LANGUAGES

(Common *to DECS & VLSI S.D*)

Max. Marks: 60 **Time: 03 Hours**

****

Answer *any five* questions

All Questions carry equal marks (12 Marks each)

1. a. Describe synthesis flow in verilog with suitable diagram.

   b. Explain variables and logic value sets in verilog HDL with suitable examples.

2. a. How delays can be modeled in verilog explain with suitable examples?

   b. Explain inertial delay effects and pulse rejection.

3. a. Explain with behavioral statements used in verilog with suitable examples.

   b. Briefly explain about the constructs for activity flow control.

4. a. Explain technology mapping and shared resources?

   b. Explain the synthesis of edge-triggered shift registers and counters.

5. a. Explain the synthesis of specify blocks and compiler directives.

   b. What are the benefits of the synthesis? Discuss about three state buffers.

6. a. Explain the switch level models of MOS transistors.

   b. What is signal strength and resolution of signal strength?

7. a. Explain the elements of VHDL with examples.

   b. Compare signal and variables with examples.

8. Write notes on

   a. Loop statement.
   b. Next statement.
   c. Wait statement.