Code No: 1PC315 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

FPGA ARCHITECTURES & APPLICATIONS

(Common to ES and VLSISD)

(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. Implement BCD to seven-segment code conversion using PLA and PAL.

2. a) What are the functions of logic and I/O blocks in FPGA architecture?

   b) Explain in detail about design flow of FPGA.

3. With neat sketch explain the embedded array block in XC-4000 chip.

4. a) Explain the design steps in FSM.

   b) Implement the following state table.

Present State	Next-State		Outputs						
	W=0	W=1	Z1	Z2	Z3	Z4	Z5	Z6	Z7
A(00)	A	B	0	0	0	0	0	0	0
B(01)	C	C	0	0	1	0	0	1	0
C(10)	D	D	1	0	0	1	0	0	0
D(11)	A	A	0	1	0	0	1	0	1

5. a) Write short notes on the properties of petrinets.

   b) Design traffic light controller using petrinets.

6. a) What are the advantages of One- Hot method in state machine design?

   b) Design serial 2's complementer using One-Hot method.

7. a) List various components considered in designing architecture.

   b) Design FSM centered around a 4-bit universal shift register.

8. Explain the design and implementation sequence for parallel adder on FPGA.

* * *

Code No: 1PA411 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

ADVANCED COMPUTER ARCHITECTURE

(Common to DECS & ES)

(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) Discuss in detail about processor performance?
   b) Write the different classes of computers.
2. a) Explain about data hazards?
   b) Write role of computers.
3. Write the advance technique for instruction delivery and speculation.
4. a) Explain dynamic scheduling.
   b) What are hardware box speculations?
5. Discuss in detail about virtual memory and its protections.
6. a) Explain disturbed shared memory.
   b) Write a short note on synchronization and multithreading.
7. a) Discuss the Bench marking in designing in storage devices..
   b) Explain different types of Buses.
8. a) Discuss the practical issues in interconnecting N/W's
   b) Explain designing a Cluster.

* * *

Code No: 1PB311 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. I Semester Regular Examinations, April/May 2012
EMBEDDED SYSTEM CONCEPTS
(Common to ES and VLSI SD)
(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) With a neat block diagram, explain the main components of embedded system hardware. And also list the important characteristics and constraints of embedded system.

   b) Write short notes on software for device drivers and device management in an operating system.

2. a) List all the structural units and functions of a general purpose processor.

   b) Explain how allocation of memory is done to program cache and memory management links.

3. a) Write short notes on UART.

   b) Explain CPU bus and bus protocols. Explain the elements of the ARM AMBA bus system.

4. a) Explain the two styles of inter-process communication.

   b) Explain the problem of sharing data by multiple tasks and routines.

5. a) Why do we use host system for most of the development? What are the software tools needed at the host?

   b) Explain the software–hardware trade-off? What are the advantages and disadvantages of software implementation instead of hardware implementation?

6. Explain design issues in hardware – software design and co-design?

7. a) Briefly describe the difference between waterfall and spiral development Models?

   b) Write short notes on SDL specification language? Draw an AND state in state charts?

8. Describe a design example for Automatic Chocolate Vending machine?

* * *

Code No: 1PB312 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. I Semester Regular Examinations, April/May 2012
MICRO CONTROLLERS AND INTERFACING
(EMBEDDED SYSTEMS)
(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) List the features of 8051 microcontroller?
   b) Write an ALP to copy the value 55h into the RAM memory location staring at the address 40h to 45h using
      i) Direct addressing mode.
      ii) Register indirect addressing mode without a loop.
      iii) Register indirect addressing mode with a loop.

2. a) List the four parts of 8051 and explain the dual role of port 0 and port 2.
   b) Write a program to get the x value from P1 and send x^2 to P2 continuously.
   c) Write a program to create a square wave of 66% duty cycle on bit3 of port1.

3. Describe keyboard-cum display controller (8279).

4. a) How do we measure temperature, current, voltage using MCU based measuring instruments?
   b) Write a short note on ROBOTICS and Embedded control.

5. Briefly explain about the architecture of 68HC11 controller with neat sketches.

6. a) What is the role of program counter in accessing memory?
   b) How is register file structured and memory is addressed?

7. a) What interrupt handling role is served by the order of the interrupts in the polling routine?
   b) Explain the ADC characteristic related to PIC microcontroller for
      i) $V_{ref} = V_{DD}$ and ii) for external V_{ref}

8. a) Explain ARM architecture in brief.
   b) Discuss about the 32/16 – bit ARM instruction set.

* * *

Code No: 1PB412

R11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

REAL TIME OPERATING SYSTEMS

(EMBEDDED SYSTEMS)

(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. Explain file I/O system in detail.

2. Explain about a reference model of real time systems.

3. a) Give the complete analysis of a typical real time application.

   b) Explain about soft real time systems.

4. a) Distinguish offline and online scheduling.

   b) Draw the schematic diagram of a real time system and explain its structure.

5. Explain commercial real time operating system in detail.

6. Explain about integrated failure conditions with examples.

7. Explain the following.
   a) Shell programming.
   b) System programming.

8. Explain the various context switches in detail.

* * *

Code No: 1PC311 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

VLSI TECHNOLOGY

(Common to ES and VLSISD)
(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) Give the classification of integrated circuits. What are the advantages of ICs over discrete components? List out the advantages of VLSI. [6M]
   b) List out the different fabrication procedures for MOS, CMOS and Bi-CMOS technologies and tabulate the differences. [6M]
2. a) Derive the expressions for I_{ds} versus V_{ds} of nMOS transistor in different regions of operation. [6M]
   b) Prepare the comparison table of design consideration of MOS, CMOS and Bi-CMOS inverters. [6M]
3. a) What is meant by Layout Design? Give the available software tools for layout design. Write short notes on wires and Vias. [6M]
   b) Explain how scalable design rules can be considered for effective layout design. [6M]
4. a) Explain the design approach for static complementary gates using switch logic. Also give the procedure for their delay calculations. [6M]
   b) Draw the circuit diagrams for low power gates and explain how they are called as low power gates. Give their delay calculations. [6M]
5. Consider a simple combinational logic network using switch logic and explain interconnect and layout design considerations and delay calculations. [12M]
6. Explain the design considerations, design validation and testing procedures relevant to sequential subsystem design. Consider an example of memory array. [12M]
7. a) Define and explain the terms 'Power distribution' and 'Clock distribution' relevant to floor planning methods. [6M]
   b) Explain architecture for low power Embedded CPU's with neat schematic diagram. [6M]
8. Write notes on any TWO of the following relevant to CAD systems and Chip Design. 2 x 6 = 12M
   a) Layout synthesis.
   b) Chip design methodology.
   c) Scheduling and printing.

* * *