Code : 1PB312

R11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

MICRO CONTROLLERS AND INTERFACING

(Embedded Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Explain the following instructions with an example for all possible situations.
   i) DAA ii) CJNE A, direct, relative address iii) SUBB A,@r_0
   b) Find the contents of an accumulator & PSW after the execution of the following instructions. Assume A=25h & C=1 before execution
   MOV A, #25h
   ADD A, #52h
   SUBB A, #50h
   ADDC A, 0fch
2. a) Assume a switch is connected to pin P 1.7 . Write a program to monitor its status & send two messages to serial port continuously as follows.
   Sw=0 send "NO"
   Sw=1 send "YES"
   Assume XTAL=11.0592 MHz, 9600 Baud rate, 8 bit data & 1 stop bit.
3. a) Explain the switch Debouncing routine.
   b) Describe IEEE488 bus signals & timings.
4. a) Explain control of a DC motor current and direction using internal PWM in an MCU.
   b) How can we use the incremental shaft angle encoder to measure the motor speed every second?
5. Briefly explain about the architecture of 68HC11 controller with neat sketches.
6. a) Compare Intel 8051 & PIC microcontroller.
   b) Assume that a 16-bit accumulator made up of RAM bytes called ACC16H, ACC16L has been defined. Show the instructions to add a 16-bit number NUM16H, NUM16L to the contents of accumulator, leaving the result in the accumulator & setting the C and Z bits appropriately. Minimize program words.
7. a) What is interrupt? How interrupt occurs? Explain interrupt logic.
   b) Explain UART's data handling circuitry with the help of diagram.
8. a) Discuss about the 32/16 bit ARM instruction set.
   b) Explain about ARM programming model with neat sketches.

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

REAL TIME OPERATING SYSTEMS

(Embedded Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. Explain about System V IPC in detail.

2. a) Distinguish hard and soft real time systems.

   b) Explain about periodic task model in detail.

3. Explain the following

   a) Processors and Resources.
   b) Precedence constraints and data dependency.

4. a) Distinguish between dynamic and state systems.

   b) Precedence constraints and data dependency.

5. Explain commercial real time operating systems in detail.

6. a) Explain hardware and software redundancy with examples.

   b) Explain about various scheduling mechanisms.

7. Explain about core RT Linux in detail.

8. Explain memory management task state transition system with the help of a diagram

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(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

VLSI TECHNOLOGY

(Common to ES & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1.	a)	Explain different Masking steps involved in P-well CMOS fabrication process with appropriate diagrams.	10M
	b)	Explain thermal aspects of MOS & CMOS process	2M
2.	a)	Explain the operation of Bi-CMOS inverter.	8M
	b)	Discuss the effect of latch-up in CMOS circuits.	4M
3.	a)	Give lambda based design rules for transistor design and wires.	6M
	b)	Draw and explain stick diagram & Layout of CMOS inverter.	6M
4.	a)	Explain alternatives of Gate circuits.	8M
	b)	Explain how crosstalk is major component of delay in RC wires.	4M
5.	a)	What is simulation? Explain through an example types of simulators used in combinational logic design.	6M
	b)	Discuss Power Optimization in combinational logic networks.	6M
6.	a)	Explain testing of sequential systems with appropriate examples.	8M
	b)	Discuss how sequential design is validated.	4M
7.	a)	Explain different architectures for reducing power consumption.	8M
	b)	Explain different elements SOC.	4M
8.	a)	Explain the methods of Hardware/Software Co-design.	4M
	b)	Explain paths for timing analysis and discuss false path in a barrel shifter.	8M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

DIGITAL IC DESIGN

(Common to ES & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Explain the dynamic behavior of CMOS Inverter.

   b) Explain the propagation delays of CMOS Inverter.

2. Design full adder with minimum number of Transistors using Domino logic.

3. a) What are the main factors to consider when decreasing the size of transistor?

   b) Why low power design? What are the ways to achieve the low power designs?

4. a) Explain leakage currents in DRAM cells and refresh operations.

   b) Explain the operations of CMOS SRAM cell.

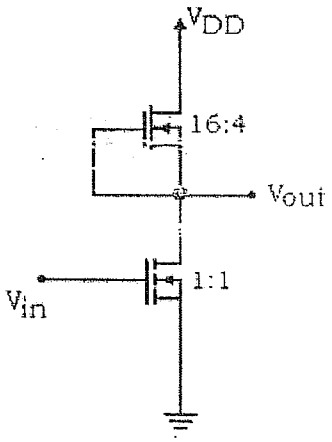
5. Design and explain the Bi-CMOS NAND gate.

6. a) What is the need of Design rules?

   b) Design a layout for CMOS.

7. a) Explain the concept of Sheet Resistance.

   b) Find total on resistance of the given circuit.



8. Draw and give the design approach for a carry look ahead adder with its structure.

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

EMBEDDED SYSTEM CONCEPTS

(Common to DECS, ES and VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Draw the functional block diagram of a basic embedded system and explain the functions of each block.

   b) Write note on classification of embedded systems?

2. Explain how processor selection and memory selection are done while designing embedded system?

3. Explain in detail about parallel communication networks using ISA, PCI and PCI-X buses.

4. Explain the various techniques used in embedded system to implement inter process communication?

5. What is meant by requirement analysis? Explain in detail how system analysis and Architecture design is done?

6. Describe embedded system design and co-design issues in the system development processes?

7. What are the features of simulator? What is its role in embedded system design? What are its possible inabilities?

8. Describe a design example for automatic chocolate vending machine?

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

FPGA ARCHITECTURES & APPLICATIONS

(Common to Embedded Systems & VLSI SD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. Explain different programming logic devices and list the differences.
2. a) Explain FPGA architecture with necessary diagrams.
   b) Write short notes on technology mapping for FPGA.
3. Draw and explain Altera Flex 10K FPGA architecture in detail.
4. a) Discuss the problems of initial state assignment for one hot encoding.
   b) Design the following using ONE-HOT encoding.

Present State	Next state		Outputs						
	W=0	W=1	Z1	Z2	Z3	Z4	Z5	Z6	Z7
A	A	B	0	0	0	0	0	0	0
B	C	C	0	0	1	0	0	1	0
C	D	D	1	0	0	1	0	0	0
D	A	A	0	1	0	0	1	0	1

5. a) Write basic concepts of petrinets.
   b) Write short notes on link state machines.
6. Explain the functional partitions for the parallel to serial adder/subtractor with necessary diagrams.
7. a) Give the model for architecture centered around a non-registered PLD.
   b) Design FSM centered around parallel loadable up/down counter.
8. Explain the design and implementation sequence for multipliers on FPGA.

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