Code No: 1PC315 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

FPGA ARCHITECTURES & APPLICATIONS

(Common to ES and VLSISD)

(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. Implement BCD to seven-segment code conversion using PLA and PAL.

2. a) What are the functions of logic and I/O blocks in FPGA architecture?

   b) Explain in detail about design flow of FPGA.

3. With neat sketch explain the embedded array block in XC-4000 chip.

4. a) Explain the design steps in FSM.

   b) Implement the following state table.

Present State	Next-State		Outputs						
	W=0	W=1	Z1	Z2	Z3	Z4	Z5	Z6	Z7
A(00)	A	B	0	0	0	0	0	0	0
B(01)	C	C	0	0	1	0	0	1	0
C(10)	D	D	1	0	0	1	0	0	0
D(11)	A	A	0	1	0	0	1	0	1

5. a) Write short notes on the properties of petrinets.

   b) Design traffic light controller using petrinets.

6. a) What are the advantages of One- Hot method in state machine design?

   b) Design serial 2's complementer using One-Hot method.

7. a) List various components considered in designing architecture.

   b) Design FSM centered around a 4-bit universal shift register.

8. Explain the design and implementation sequence for parallel adder on FPGA.

* * *

Code No: 1PC313

R11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

DIGITAL IC DESIGN

(VLSI SYSTEM DESIGN)

(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) Explain VTC characteristics of CMOS inverter?

   b) Derive an expression for the gain and noise margins, assuming that PMOS and NMOS are long channel devices (or) the supply voltages are low.

2. a) What are the advantages of Domino logic? Draw Domino OR gate and explain its operation with suitable wave-forms.

   b) Derive the Rise Time equation of CMOS Inverter.

3. a) Explain different types of power dissipations with examples.

   b) Explain about low power design through voltage scaling.

4. a) Explain the memory structure of SRAM cell with read write operation.

   b) Design the single bit adder with minimum number of transistors.

5. a) Explain the static behavior of Bi-CMOS circuit.

   b) Explain the switching delay in Bi-CMOS logic circuits.

6. a) Explain different types of wiring capacitances.

   b) Write the design rules for metal layers and contacts.

7. Design a layout for the given expression $F = A\overline{(CD + B)}$.

8. a) Give the subsystem design consideration of a 4-bit adder.

   b) Explain step by step subsystem design approach, consider adder as an example.

* * *

Code No: 1PB311 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. I Semester Regular Examinations, April/May 2012
EMBEDDED SYSTEM CONCEPTS
(Common to ES and VLSI SD)
(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) With a neat block diagram, explain the main components of embedded system hardware. And also list the important characteristics and constraints of embedded system.

   b) Write short notes on software for device drivers and device management in an operating system.

2. a) List all the structural units and functions of a general purpose processor.

   b) Explain how allocation of memory is done to program cache and memory management links.

3. a) Write short notes on UART.

   b) Explain CPU bus and bus protocols. Explain the elements of the ARM AMBA bus system.

4. a) Explain the two styles of inter-process communication.

   b) Explain the problem of sharing data by multiple tasks and routines.

5. a) Why do we use host system for most of the development? What are the software tools needed at the host?

   b) Explain the software–hardware trade-off? What are the advantages and disadvantages of software implementation instead of hardware implementation?

6. Explain design issues in hardware – software design and co-design?

7. a) Briefly describe the difference between waterfall and spiral development Models?

   b) Write short notes on SDL specification language? Draw an AND state in state charts?

8. Describe a design example for Automatic Chocolate Vending machine?

* * *

Code No: 1PC312 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

ANALOG IC DESIGN

(VLSI SYSTEM DESIGN)

(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) Explain the different regions of operation in a MOS transistor.

   b) Write a note on MOS models.

2. a) State the limitations of single stage amplifiers.

   b) Explain common source amplifier with current mirror active load.

3. a) Discuss about various OPAMP compensation techniques.

   b) Explain High output impedance current Mirrors.

4. a) Explain Bi-CMOS comparator with a neat circuit diagram.

   b) Discuss in detail the design features of folded cascade operational amplifier.

5. a) Explain about CMOS and Bi-CMOS sample and hold circuits and compare.

   b) Explain the basic operation and analyze switched capacitor circuits.

6. a) Design a second order high pass butterworth filter with a cut off frequency of 1 KHz and a passband gain of –2. Assume that a 5V power supply and CMOS clock are used.

   b) Explain briefly about correlated double sampling techniques.

7. a) With the help of a neat circuit diagram and waveforms, explain the operation of a cyclic flash type ADC. What are its special features?

   b) What are the performance limitations of data converters?

8. a) What is over sampling? Explain over sampling with and without noise sampling.

   b) Discuss in detail about high order modulators.

* * *

Code No: 1PC314 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

HARDWARE DESCRIPTION LANGUAGES

(Common to DECS and VLSISD)

(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) In verilog, explain behavioral descriptions?
   b) Explain data types and data objects in verilog HDL with suitable examples.

2. a) What is a net delay and propagation delay explain in verilog HDL?
   b) Explain the user defined primitives.

3. Explain the following with example.
   a) Delay-blocked assignment.
   b) Intra assignment.

4. a) What is technology-independent design? Explain?
   b) Explain hierarchical structures and design partitions.

5. a) Explain the synthesis of user defined tasks and functions.
   b) Explain the restrictions on synthesis of 'X' and 'Z' with suitable examples?

6. a) Explain the switch level models of static CMOS circuits.
   b) Write about CMOS transmission Gates.

7. a) Explain VHDL subprograms with examples.
   b) Explain VHDL operators with examples.

8. Write notes on
   a) Process statement.
   b) Report statement.
   c) Assertion statement.

* * *

Code No: 1PC311 **R11**

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, April/May 2012

VLSI TECHNOLOGY

(Common to ES and VLSISD)
(For students admitted in 2011-12)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks

* * * * *

1. a) Give the classification of integrated circuits. What are the advantages of ICs over discrete components? List out the advantages of VLSI. [6M]
   b) List out the different fabrication procedures for MOS, CMOS and Bi-CMOS technologies and tabulate the differences. [6M]
2. a) Derive the expressions for I_{ds} versus V_{ds} of nMOS transistor in different regions of operation. [6M]
   b) Prepare the comparison table of design consideration of MOS, CMOS and Bi-CMOS inverters. [6M]
3. a) What is meant by Layout Design? Give the available software tools for layout design. Write short notes on wires and Vias. [6M]
   b) Explain how scalable design rules can be considered for effective layout design. [6M]
4. a) Explain the design approach for static complementary gates using switch logic. Also give the procedure for their delay calculations. [6M]
   b) Draw the circuit diagrams for low power gates and explain how they are called as low power gates. Give their delay calculations. [6M]
5. Consider a simple combinational logic network using switch logic and explain interconnect and layout design considerations and delay calculations. [12M]
6. Explain the design considerations, design validation and testing procedures relevant to sequential subsystem design. Consider an example of memory array. [12M]
7. a) Define and explain the terms 'Power distribution' and 'Clock distribution' relevant to floor planning methods. [6M]
   b) Explain architecture for low power Embedded CPU's with neat schematic diagram. [6M]
8. Write notes on any TWO of the following relevant to CAD systems and Chip Design. 2 x 6 = 12M
   a) Layout synthesis.
   b) Chip design methodology.
   c) Scheduling and printing.

* * *