Code : 1PC315

R11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

FPGA ARCHITECTURES & APPLICATIONS

(Common to Embedded Systems & VLSI SD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. Explain different programming logic devices and list the differences.
2. a) Explain FPGA architecture with necessary diagrams.
   b) Write short notes on technology mapping for FPGA.
3. Draw and explain Altera Flex 10K FPGA architecture in detail.
4. a) Discuss the problems of initial state assignment for one hot encoding.
   b) Design the following using ONE-HOT encoding.

Present State	Next state		Outputs						
	W=0	W=1	Z1	Z2	Z3	Z4	Z5	Z6	Z7
A	A	B	0	0	0	0	0	0	0
B	C	C	0	0	1	0	0	1	0
C	D	D	1	0	0	1	0	0	0
D	A	A	0	1	0	0	1	0	1

5. a) Write basic concepts of petrinets.
   b) Write short notes on link state machines.
6. Explain the functional partitions for the parallel to serial adder/subtractor with necessary diagrams.
7. a) Give the model for architecture centered around a non-registered PLD.
   b) Design FSM centered around parallel loadable up/down counter.
8. Explain the design and implementation sequence for multipliers on FPGA.

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(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

Hardware Description Languages

(Common to DECS & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Write about different Descriptive Styles in HDL. 5M

   b) Explain about Structural (Top-Down) Design Methodology 7M

2. a) Give the Verilog Models for Gate Propagation Delay (Inertial Delay) and Net Delay (Transport Delay). 6M

   b) Write some of the user defined primitives required to model both combinational and sequential circuit. 6M

3. a) Explain how to describe the Behavioral Model of Finite State Machines. 6M

   b) Write about Intra Assignment Delay and inter assignment delay. Explain with suitable example. 6M

4. a) What is the difference between simulation and synthesis? What are the benefits of synthesis? 6M

   b) What are the various styles for synthesizing Combinational Logic circuits? 6M

5. a) Write about Timings Controls in Synthesis. 6M

   b) Define task and function.Write about Synthesis of User-Defined Tasks and Synthesis of User-Defined Functions. 6M

6. a) What is the difference between static and dynamic CMOS circuits? Write the Verilog code for switch level CMOS NAND gate. 7M

   b) What are the various signal Strength levels. Explain how to reduce signal strength by Primitives. 5M

7. a) Draw VHDL Top-Down Design methodology and explain. 8M

   b) What are the various operators used in VHDL. 4M

8. a) Write some of the data types used in Verilog. 4M

   b) Write the syntaxes for the following Sequential statements: Wait, if, case, loop, next, exit, return, null. 8M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

VLSI TECHNOLOGY

(Common to ES & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1.	a)	Explain different Masking steps involved in P-well CMOS fabrication process with appropriate diagrams.	10M
	b)	Explain thermal aspects of MOS & CMOS process	2M
2.	a)	Explain the operation of Bi-CMOS inverter.	8M
	b)	Discuss the effect of latch-up in CMOS circuits.	4M
3.	a)	Give lambda based design rules for transistor design and wires.	6M
	b)	Draw and explain stick diagram & Layout of CMOS inverter.	6M
4.	a)	Explain alternatives of Gate circuits.	8M
	b)	Explain how crosstalk is major component of delay in RC wires.	4M
5.	a)	What is simulation? Explain through an example types of simulators used in combinational logic design.	6M
	b)	Discuss Power Optimization in combinational logic networks.	6M
6.	a)	Explain testing of sequential systems with appropriate examples.	8M
	b)	Discuss how sequential design is validated.	4M
7.	a)	Explain different architectures for reducing power consumption.	8M
	b)	Explain different elements SOC.	4M
8.	a)	Explain the methods of Hardware/Software Co-design.	4M
	b)	Explain paths for timing analysis and discuss false path in a barrel shifter.	8M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET

(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

ANALOG IC DESIGN

(VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

* * * * *

1. a) Compare and contrast the CS, CG and CD amplifiers.

   b) Give high frequency equivalent circuit of n-channel MOSFET. Explain.

2. a) Explain large signal modeling of a single stage BJT amplifier with neat sketches.

   b) Draw the circuit of a simple CMOS current mirror and explain its working principle.

3. a) Give frequency response of an opamp and explain.

   b) Explain common gate amplifier with current mirror active load.

4. a) What is the need for compensating networks in opamps and explain about current mirror compensating network.

   b) Discuss about

      i) Latched and Bi-CMOS comparators

      ii) Charge injection error

5. a) Explain about Bi-CMOS sample and hold circuit with relevant waveforms.

   b) Explain and give the design procedure of Biquard switched capacitor filter.

6. a) What is a switched capacitor filter? List important features of it.

   b) Explain in detail about switched capacitor gain circuit.

7. a) Explain the following with reference to ADC:

      i. Conversion time

      ii. Accuracy

      iii. Resolution time

      iv. Quantization time

   b) Discuss about Nyquist rate D/A converters.

8. Write short notes on the following

      i. Digital decimation filter

      ii. Band pass over sampling converter.

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(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

DIGITAL IC DESIGN

(Common to ES & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

* * * * *

1. a) Explain the dynamic behavior of CMOS Inverter.

   b) Explain the propagation delays of CMOS Inverter.

2. Design full adder with minimum number of Transistors using Domino logic.

3. a) What are the main factors to consider when decreasing the size of transistor?

   b) Why low power design? What are the ways to achieve the low power designs?

4. a) Explain leakage currents in DRAM cells and refresh operations.

   b) Explain the operations of CMOS SRAM cell.

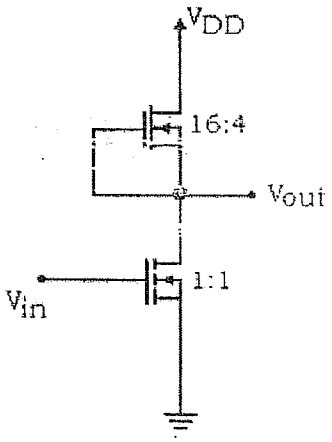
5. Design and explain the Bi-CMOS NAND gate.

6. a) What is the need of Design rules?

   b) Design a layout for CMOS.

7. a) Explain the concept of Sheet Resistance.

   b) Find total on resistance of the given circuit.



8. Draw and give the design approach for a carry look ahead adder with its structure.

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(AUTONOMOUS)

M.Tech. I Semester Regular Examinations, February 2014

EMBEDDED SYSTEM CONCEPTS

(Common to DECS, ES and VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Draw the functional block diagram of a basic embedded system and explain the functions of each block.

   b) Write note on classification of embedded systems?

2. Explain how processor selection and memory selection are done while designing embedded system?

3. Explain in detail about parallel communication networks using ISA, PCI and PCI-X buses.

4. Explain the various techniques used in embedded system to implement inter process communication?

5. What is meant by requirement analysis? Explain in detail how system analysis and Architecture design is done?

6. Describe embedded system design and co-design issues in the system development processes?

7. What are the features of simulator? What is its role in embedded system design? What are its possible inabilities?

8. Describe a design example for automatic chocolate vending machine?

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