R11

Code : 1PC312

M.Tech. I Semester Supplementary Examinations, July/August 2014

Analog IC Design

(VLSI System Design)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Explain large signal modeling of single stage BJT amplifier with neat sketches	8M
	b)	Justify the choice of PMOS loads?	4M
2.	a)	Explain in detail about advanced current mirror compensations network?	6M
	b)	Briefly explain the need for compensating networks in op-amps?	6M
3.	a)	Explain different type of comparators with neat circuit diagrams?	8M
	b)	Explain about charge injection error?	4M
4.	a)	Deduce the necessary conditions that ensure zero input offset voltage for two stage op-amp?	6M
	b)	What is CMFB circuit? What are the various methods of designing CMFB circuit? And compare them?	6M
5.	a)	Explain about various performance parameters of sample and hold circuit?	6M
	b)	Draw the circuit of switched capacitor circuit and explain its principle?	6M
6.	a)	Compare and contrast CMOS and BICMOS sample and hold circuit & their performance?	6M
	b)	Discuss in detail the design features of fully differential folded cascade op-amp?	6M
7.	a)	Explain briefly a 3bit A/D converter state the salient issues in designing flash A/D converters?	6M
	b)	Explain the principle of operation of dual slope A/D converters?	6M
8.	a)	Discuss in detail the noise shaped sigma modulator?	6M
	b)	What is over Sampling? Explain over sampling with & without noise sampling?	6M

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R-11

M.Tech. I Semester Supplementary Examinations, July/August 2014

Digital IC Design
(Common to Embedded Systems and VLSI System Design)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a) Explain the CMOS Inverter Static and Dynamic characteristics
   b) Give the Description of Dynamic CMOS Inverter with its equivalent circuit diagram.
2. a) Explain about sequential circuits with suitable example.
   b) Explain the Ratioed logic of static complementary gates.
3 a) Explain about power consumption in CMOS gates.
   b) Describe and design the low power CMOS design.
4. a) Explain about CMOS memory Design.
   b) Explain the arithmetic circuit of CMOS adder with suitable example.
5. a) Differentiate between CMOS and BiCMOS design.
   b) Explain the static and Dynamic behavior of BiCMOS logic.
6. a) Explain the Design rules for the silicon Gate NMOS.
   b) Explain about wire capacitances.
7. a) Explain the lambda-based design rules.
   b) Describe about Drive Large capacitive load.
8. a) Explain with short notes on carry-look-ahead adders and multipliers.
   b) Describe in detail about the modified Booth's algorithm.

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Code : 1PB311

R11

M.Tech. I Semester Supplementary Examinations, July/August 2014

EMBEDDED SYSTEM CONCEPTS

(Common to DECS, ES and VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1. Explain Embedded System-On-Chip (SOC) and its components in detail.

2. Explain how separate caches for instruction, data and branch transfer help in speed up of a system.

3. Explain how asynchronous, synchronous and iso-synchronous communication devices are handled in embedded systems? Write note on RS232C/RS485 communication standards?

4. Write note on possible problems faced, while sharing data by multiple tasks and routines and give their solutions.

5. Describe different system design methodologies? Explain how requirement analysis is done.

6. Write a detail note on embedded software development process and tools?

7. Write note on hardware laboratory tools used in prototype development and testing of embedded system design?

8. Describe a design example for adaptive cruise control in a car?

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Code : 1PC315

R11

M.Tech. I Semester Supplementary Examinations, July/August 2014

FPGA Architectures and Applications

(Common to ES & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Draw a neat block diagram of Xilinx 3000 series I/O Block and explain each block in detail. 7M

   b) Compare PLA, PAL and PLDs with respect to different features, programming and applications. 5M

2. a) List the programming technologies of FPGA and explain in detail. 6M

   b) Explain the design flow of FPGAs. 6M

3. a) Explain about the technology mapping for FPGAs. 6M

   b) Give the Xilinx XC4000 features and compare them with Altera's Flex 8000 series FPGA. 6M

4. a) Explain the application of the one Hot method to a serial 2's complement. 6M

   b) Explain the rules for clocking in FSM design 6M

5. a) Explain the extended petrinetes for parallel controllers. 6M

   b) Explain about Linked state Machines and one-Hot state machine 6M

6. a) Develop one hot state diagram for a sequence checker whose output is '1' whenever the sequence 0101 is detected. Also specify the Transition Table. 6M

   b) With an example explain about one Hot design Method using ASMs 6M

7. Draw an ASM chart for the control network for the floating point subtractor. Define control signals used and give equations for each control signal used as an input to the control network. 12M

8. Draw an ASM chart for a binary multiplier. Design the control logic using one hot design. 12M

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R11

M.Tech. I Semester Supplementary Examinations, July/August 2014

Hardware Description Languages

(Common to DECS & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1. a) Write the differences between Structural and Behavioral Description In Verilog with an example. 6M

   b) Write about Data Types, Strings, Constants, and Operators in HDL. 6M

2. a) Design half-adder module with time delay assignment through parameter declaration. 6M

   b) Give the test bench, simulation results for the above module. 6M

3. a) What are the various delay constructs in Verilog? 4M

   b) Write syntax for Behavioral Statements, Procedural Assignment, and Procedural Continuous Assignments by taking a simple example. 8M

4. a) What is the difference between combinational and sequential logic circuits? Explain with examples. 6M

   b) Explain how to synthesize Latches, Edge-Triggered Flip Flops, Finite State Machines 6M

5. a) What is meant by synthesis of a design? How it is useful in hardware design? 6M

   b) Write about synthesis of language constructs Nets, Register Variables, Expressions and Operators. 6M

6. a) Write the differences between pass transistor logic and transmission gate logic. Draw transmission gate and write the Verilog code for it. 6M

   b) Write about Signal Strengths and Wired Logic in Switch-level models. 6M

7. a) What is VHDL? Give the importance. Write Some of the CAD tools used in VLSI. 4M

   b) Explain the terms Simulation, Optimization, Place and Route in VHDL. 8M

8. a) Write the differences between VHDL and Verilog. 5M

   b) Write VHDL code for full-adder circuit using Assertion Statements 7M

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M.Tech. I Semester Supplementary Examinations, July/August 2014

VLSI TECHNOLOGY

(Common to ES & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Explain NMOS transistor fabrication process with appropriate diagrams.	8M
	b)	Compare CMOS & Bipolar Technologies.	4M
2.	a)	Derive the expression for I_{ds} for saturated and non-saturated regions of MOS transistor.	8M
	b)	Explain Body effect of NMOS device.	4M
3.	a)	Explain encoding of NMOS process with appropriate color structures.	6M
	b)	Explain Stick diagram and layout of CMOS inverter.	6M
4.	a)	Explain different strategies for building of low-power gates.	8M
	b)	Discuss Elmore delay calculation for RC transmission line.	2M
5.	a)	Explain different techniques of Logic gates testing.	8M
	b)	Explain the use of Left-edge channel routing algorithm.	4M
6.	a)	Explain clocking discipline of sequential system.	8M
	b)	Explain power optimization in sequential systems.	4M
7.	a)	Explain different floor planning methods of a chip.	10M
	b)	What is signature analysis of LFSR?	2M
8.		Explain Placement, Global routing and Detailed routing of chip.	12M

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