Code : 1PC311

R-11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. I- Semester *Supplementary Examinations, November 2012*
VLSI TECHNOLOGY
(Common *to ES & VLSI S.D*)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a. What is Moore's law? Give the various MOS technologies trends and projections. List out the advantage of VLSI. 6M
   b. Tabulate the comparison between MOS, CMOS and BiCMOS technologies with respect to various performance parameters. 6M
2. a. Define the following MOS transistor parameters and give their expressions.
      i. Threshold voltage ii. Trans conductance
      iii. Output conductance iv. Figure of Merit. 6M
   b. Explain the concept of Latch-up in CMOS circuits with suitable diagram. 6M
3. a. Draw the various transistor structures and explain any one of their layout design procedure. 6M
   b. Explain how scalable design rules can be considered for effective layout design. 6M
4. a. Explain the design approach and delay calculations for static complementary gates using switch logic. 6M
   b. Write notes on resistive and inductive interconnect delays with suitable example. 6M
5. a. Write short notes on power optimization and testing methodology of combinational logic circuits in VLSI design. 6M
   b. Explain the layout design considerations and delay calculations of combinational logic networks with relevant example. 6M
6. With an example of a memory cell, explain the design approach, power optimization techniques and clocking disciplines of sequential subsystem design. 12M
7. a. What are the various floor planning methods available for VLSI Design? Explain any one of them in detail. 6M
   b. Explain the concept of high-level synthesis related to an architectural design. 6M
8. Write notes on any TWO of the following relevant to CAD systems and chip design
   a. Layout Analysis. 2 X 6 = 12M
   b. Hardware / Software Co-design.
   c. Scheduling and printing.

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M.Tech. I- Semester *Supplementary Examinations, November 2012*
EMBEDDED SYSTEM CONCEPTS
(Common *to ES & VLSI S.D*)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a. Explain the need of watchdog timer and reset after the watched time?

   b. What do you mean by stem-on-chip (SOC)? How will the definition of an embedded system change with SOC? What are the advantages offered by an ASIC for designing in embedded system?

2. a. What are the features that hardware designer must take into account while selecting a processors? Explain with an exemplary system?

   b. Explain how allocation of memory is done to interfacing processors?

3. a. Write short notes on RS485.

   b. Draw the processor of embedded system connected to system memory bus and networked to other subsystems through parallel bus using PCI bridge? Explain about PCI and PCI/X buses.

4. a. Explain the multiple processes in a mobile phone device application?

   b. What is a task? What are the different task states? Explain.

5. a. Why is a target system? How does the target system differ from final embedded system? What do you mean by application software for a target system?

   b. Explain issues in embedded designing.

6. Explain different laboratory tools used for embedded system.

7. a. Explain how specifications turns into overall system architecture design.

   b. Provide realistic examples of how a requirements document may be
   i. ambiguous ii. Incorrect iii. Incomplete iv. Unverifiable.

8. Describe a design example for Smart card.

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M.Tech. I- Semester *Supplementary Examinations, November 2012*

HARDWARE DESCRIPTION LANGUAGES

(Common *to DECS & VLSI S.D*)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions

All Questions carry equal marks (12 Marks each)

1. a. Describe synthesis flow in verilog with suitable diagram.

   b. Explain variables and logic value sets in verilog HDL with suitable examples.

2. a. How delays can be modeled in verilog explain with suitable examples?

   b. Explain inertial delay effects and pulse rejection.

3. a. Explain with behavioral statements used in verilog with suitable examples.

   b. Briefly explain about the constructs for activity flow control.

4. a. Explain technology mapping and shared resources?

   b. Explain the synthesis of edge-triggered shift registers and counters.

5. a. Explain the synthesis of specify blocks and compiler directives.

   b. What are the benefits of the synthesis? Discuss about three state buffers.

6. a. Explain the switch level models of MOS transistors.

   b. What is signal strength and resolution of signal strength?

7. a. Explain the elements of VHDL with examples.

   b. Compare signal and variables with examples.

8. Write notes on

   a. Loop statement.
   b. Next statement.
   c. Wait statement.