II B.Tech. I Semester Supplementary Examinations November 2019

## Digital Logic Design

( Computer Science and Engineering )
Max. Marks: 70
Time: 3 Hours
Answer all five units by choosing one question from each unit ( $5 \times 14=70$ Marks )
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## UNIT-I

1. a) Convert (2AC5.D $)_{\mathrm{H}}$ to decimal, octal and binary.
b) Explain subtraction using r-1's complements with an example.

## OR

2. a) Express the following functions as a sum of min terms and as a product of max terms: $\quad F(A, B, C)=B^{1} C+A^{1} C+B C$
b) Reduce the following Boolean expressions to the indicated number of literals using Boolean theorems.

| I. $A^{\prime} C^{\prime}+A B C+A C^{\prime}$ | to THREE literals |  |
| :--- | :--- | ---: |
| II. $A B C^{1} D+A^{1} B D+A B C D$ | to TWO literals |  |
| III. $A^{\prime} B\left(D^{\prime}+C D\right)+B\left(A+A^{\prime} C D\right)$ to ONE literal | 7 M |  |

## UNIT-II

3. a) Draw the multiple-level NAND circuit for the following expression:
$F=w(x+y+z)+x y z$
b) Implement the following Boolean expression with exclusive-OR and AND gates: $F=A B^{1} C D^{1}+A^{1} B C D^{1}+A B^{1} C^{1} D+A^{1} B C^{1} D$

## OR

4. a) Simplify the following Boolean function together with the don't care conditions and simplify into SOP form
$F(A, B, C, D)=\sum_{m}(4,5,6,7,12,13,14), d(A, B, C, D)=\sum_{m}(1,9,11,15)$
b) Make a K-map for the function $f(x, y, z, w)=x y+x z^{\prime}+z+x w+x y ’ z+x y z$ and realize the minimized expression using NAND gates only

## UNIT-III

5. a) Design a 4- bit ADDER/SUBTRACTOR circuit with add/sub control line.
b) Realize the function $f(A, B, C, D)=\sum(1,2,3,4,6,7,8,10,12,14,15)$ using
i) $8: 1 \mathrm{MUX}$
ii) 4:1 MUX
6. a) Design and draw a full subtractor which will use two half subtractors.
b) Define decoder. Construct $3 \times 8$ decoder using logic gates.

## UNIT-IV

7. a) Convert a SR flip-flop to $D$ type flip flop? 7M
b) Explain with the help of neat diagram, the operation of 3-bit bidirectional shift register.

## OR

8. a) Draw the circuit diagram of clocked D-flip flop with NAND gates and explain its operation using truth table

7M
b) Explain with the help of neat diagram, the operation of 4-bit register with
parallel load.

## UNIT-V

9. a) Show that a BCD ripple counter can be constructed using a 4-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010

## b) Derive the PLA programming table for the combinational circuit that squares a 3-bit number

## OR

10. a) Explain Ring counter operation and its applications using a diagram 7M
b) Realize the following Boolean function using PROM $F(x, y, z, w)=\Sigma_{m}(0,1,3,6,8,9,15)$.
Hall Ticket Number :

$\square$
Code: 4G236
R-14
II B.Tech. I Semester Supplementary Examinations November 2019
Electrical Engineering and Electronics Engineering
( Common to ME, CSE \& IT )
Max. Marks: 70Time: 3 HoursAnswer all five units by choosing one question from each unit ( $5 \times 14=70$ Marks )
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UNIT-I1. a) Define the Ohm's Law and its applications.7M
b) State and explain Kirchoff's laws using neat diagrams. ..... 7M
OR2. a) Derive the expression for delta to star transformation.7M
b) Two resistances of 1.5 and 3.5 are connected in parallel and their combination is connected is series with a resistance of 1.95 . Find the equivalent resistance of the circuit. What current will it draw if connected to a 30V supply?

## UNIT-II

3. a) A 6 pole, lap wound armature has 840 conductors and flux per pole of 0.018 wb . Calculate the emf generated when the machine is running at 600rpm.
b) Explain the operation \& principle of dc motors and explains the significance of back emf in dc motors. ..... 7M
OR4. Explain classification of a DC generator along with suitable diagrams and voltageand current relationship.
UNIT-III5. a) Derive the expression for E.M.F equation of a transformer.7M
b) Explain the principle operation of a three phase induction motor with relevant diagrams ..... 7M
OR
4. a) Describe the tests that can be performed on a single phase transformer in detail. ..... 7M
b) A 3-Ф induction motor runs at 1200 rpm at no load and 1140 rpm at full load when supplied with power from a 60 Hz , 3 phase line. Calculate number of poles and slip at full load. ..... 7M
UNIT-IV
5. Explain the operation of Half wave rectifier with relevant diagrams.14M
OR
6. a) Construct the practical circuit of a transistor and elaborate it. ..... 7M
b) Explain the operation of transistor as an amplifier. ..... 7M
UNIT-V9. Describe how phase and frequency are measured by using Lissajous figures.14M
OR
7. Explain the Block diagram of CRO with a neat sketch. ..... 14M
