Hall Ticket Number :										

R-14

Code: 4G236

II B.Tech. I Semester Supplementary Examinations May 2019

Electrical Engineering and Electronics Engineering

(Common to ME, CSE & IT)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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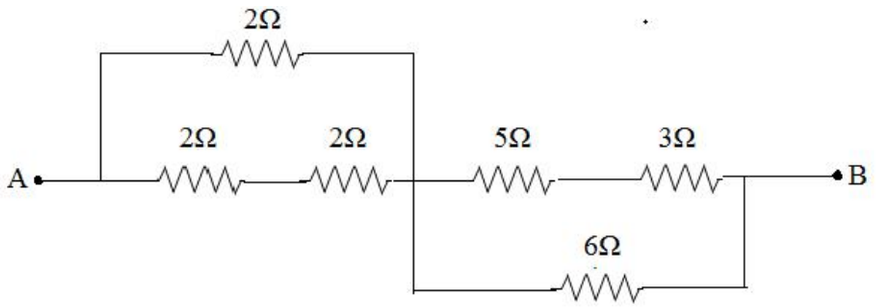
UNIT–I

1. a) Define the following i) Resistance ii) Inductance iii) Capacitance. Also give the V-I relationship for the above elements.

   b) Find the equivalent resistance between A & B terminals.



OR

2. a) Derive the expression for star to delta transformation.

   b) Two resistors of each 4Ω and 2Ω are connected in parallel across a 10V DC supply. Find the current through each resistor by current division technique.

UNIT–II

3. a) Explain the operation of principle of DC generator.

   b) Derive the expression for Torque in a DC Motor.

OR

4. a) Explain the speed control methods of a DC shunt motor.

   b) Elaborate about Swinburne's test on dc machine.

UNIT–III

5. A 400V, 10KVA, 3-Φ alternator with star connected stator winding has an effective armature resistance per phase of 1.0 Ω. The alternator generates an open circuit voltage per phase is 90V with a field current of 1.0A. During the short circuit test, with 1.0A of field current the short circuit current flowing in the armature is 15A. Calculate

   The synchronous impedance B) Synchronous reactance

OR

6. a) Explain the principle of operation of single phase Transformer with neat sketch.

   b) Explain Torque-Slip Characteristics of a Three phase induction motor.

UNIT–IV

7. Explain the operation of Bridge rectifier with relevant diagrams.

OR

8. a) Explain the operation of P-N junction diode mentioning its applications.

   b) Explain the input and output characteristics of transistor in CE configuration.

UNIT–V

9. Enumerate the applications of dielectric heating and induction heating.

OR

10. a) Describe how voltage, current and time period are measured by using CRO.

    b) List the applications of CRO.

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Hall Ticket Number :										

R-14

Code: 4G132

II B.Tech. I Semester Supplementary Examinations May 2019

Digital Logic Design

(Common to CSE & IT)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) i) Convert $(4057.06)_8$ to binary code.
   ii) What is reflection code? Give Example 7M
   b) i) Perform the subtraction in Excess-3 code using the 10's complement method: 597-239.
   ii) State De Morgan's theorem for three variables 7M

OR

2. a) i) Prove that $\left(\overline{A+\overline{BC}}\right)\left(A\overline{B}+\overline{ABC}\right)=\overline{A}BC$.
   ii) Implement OR Gate using NAND Gates 7M
   b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB
   ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M

UNIT–II

3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = ∑(1, 3, 4, 5, 6, 7, 9, 12, 13) 10M
   b) Show that the dual of the exclusive-OR is equal to its complement 4M

OR

4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates:
   F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M
   b) Minimize the function f = Σ m(0,2,4,6,7,8,10,12,13,15) using K-Map and obtain SOP form of it 7M

UNIT–III

5. a) Design 4-bit binary to Gray code converter. 7M
   b) Implement the function f(A,B,C)= $\Sigma m(0,2,5,7)$ using 4x1 MUX. 7M

OR

6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M
   b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M

UNIT–IV

7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M
   b) What is difference between latch and flip flop? Explain about clocked RS flip flop using NAND gates 7M

OR

8. a) With a neat diagram, explain master slave JK Flip Flop 7M
   b) Explain the operation of universal shift register. 7M

UNIT–V

9. a) Draw and explain the operation of 4 bit ring counter. 7M
   b) i) Compare PLA with PROM.
   ii) What is ROM? List the different types of ROMs 7M

OR

10. a) Draw and explain 4-bit Johnson counter using D-flip flop. 7M
    b) Implement the following functions using PLA.
    A (x,y,z)= ∑m (1,2,4,6)
    B (x,y,z) = ∑m (0,1,6,7)
    C (x,y,z) = ∑m (2,6) 7M

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