	Ticket Nur	mbori									
										R-17	]
Code	: 7GC32 ∥ B.Te	ch. I Semes	ster Su	opleme	entar	v Fxar	nina	tions	Mav 2	019	-
	1 0.10		-	ring M						.017	
			•	imon to							
	. Marks: 70				antian	frama		unit ( E		Time: 3 Hours	
4		ve units by cł	loosing	one qu	*****	nome	acht	uni ( S	x 14 –	/U/MAIKS J	
				U	I-TIV						
1. a)	Find a re	al root of the	equation	on $x^3 - 2$	2x - 5 =	0 usir	ng bis	ection	metho	d correct to	
	three dec	cimal places.									7M
b)	Find the	real root of th	e equat	tion sin <sup>2</sup>	x + 1 =	$x^2$ usin	g Nev	wton-R	aphso	n method.	7M
					OR						
2. a)	Employ I	Euler's metho	od to o	btain th	e app	roxima	te va	lue of	yat x	=1.0 for the	
differential equation $\frac{dy}{dx} = x - y^2$ , $y(0) = 1$ .											
$dx = x^{-x} y^{-x}, y^{-1}$											7M
b) Apply Runge-Kutta method of order 4, compute $y(0.2)$ and $y(0.4)$ from the											
equation $\frac{dy}{dx} = x + y$ , $y(0) = 1$ .											7M
				UN	IIT–II						
3. a)	The popu	ulation of a to	wn in th	e decer	nial ce	ensus	was g	iven b	elow		
		Year :	x	1891	190	1 19	11	1921	1931	I	
		Populatio	•	46	66	8	1	93	101		
		(in thousa	/								714
		the populatio		-							7M
b)	-	ange's interp	olation	formula	to find	the va	lue of	fywh	en x = 3	3.5 from the	
	following	table									
			<i>x</i>	0	1	3	4	_			
			У	-12	0	12	24				7M
					OR						

4. a) Find the first and second derivatives of the function tabulated below at the point x = 1.5

x	1.5	2.0	2.5	3.0	4.0	
у	3.375	7.0	13.625	38.875	59	7M

b) Evaluate  $\int_{0}^{1} \frac{dx}{1+x^2}$  by using

(i)Trapezoidal rule (ii)Simpson's  $\frac{1}{3}$  rule and (iii)Simpson's  $\frac{3}{8}$  rule with h = 0.5 and 0.125 7M

7M

7M

#### UNIT–III

5. a) Determine the values of *a* and *b* by the method of least squares such that  $y = ae^{bx}$  fits the following data

x	2	4	6	8	10	
У	4.077	11.084	30.128	81.897	222.62	7M

b) Solve  $(p^2 + q^2)y = qz$  using Charpit's method.

$\sim$	n
	ĸ
-	•••

6. a) Fit a second degree polynomial to the following data by the method of least squares

X	10	12	15	23	20
у	14	17	23	25	21

b) Using the method of separation of variables,

solve 
$$\frac{\partial u}{\partial x} = 4 \frac{\partial u}{\partial y}$$
, when  $u(0, y) = 8e^{-3y}$ 

7. Prove that  $x^2 = \frac{f^2}{3} + 4\sum_{n=1}^{\infty} (-1)^n \frac{\cos nx}{n^2}$ , -f < x < f by using Fourier series and hence show that  $\sum_{n=1}^{\infty} \frac{1}{n^2} = \frac{f^2}{6}$  14M

#### OR

8. Obtain a half range cosine series for  $f(x) = \begin{cases} kx, 0 \le x \le l/2 \\ k(l-x), l/2 \le x \le l \end{cases}$ 

and deduce the sum of the series is 
$$\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + ... = \frac{f^2}{8}$$
  
**UNIT-V**

# 9. Find the Fourier sine and cosine transforms of $e^{-ax}(a > 0)$ . Hence Evaluate the integrals $\int_{0}^{\infty} \frac{x \sin x}{x^{2} + a^{2}} dx$ and $\int_{0}^{\infty} \frac{\cos x}{x^{2} + a^{2}} dx$ 14M

OR

10. Obtain the Fourier sine transfromation of

$$f(x) = \begin{cases} 4x, & \text{for } 0 < x < 1\\ 4-x, & \text{for } 1 < x < 4\\ 0, & \text{for } x > 4 \end{cases}$$
14M

Hall	Tick	xet Number :										
Code	<u>م. مر</u>	C131 R-17										
Code	<b>;</b> . /G	II B.Tech. I Semester Supplementary Examinations May 2019 Advanced Data Structures Through C++ ( Computer Science and Engineering )										
		arks: 70 Time: 3 Ho ver all five units by choosing one question from each unit ( 5 x 14 = 70 Marks ) *********	ours									
1.	a)	<b>UNIT–I</b> What are the static class members? Explain each in detail.	9M									
	b)	How access control is provided in C++.	5M									
	OR											
2.	a)	Define class scope. Explain this concept with an example.	7M									
	<ul> <li>b) C++ provides a mechanism in which non-member can have access to private member of a class. Justify?</li> </ul>											
		UNIT–II										
3.	a)	Identify the purpose of operator overloading and demonstrate operator										
	L.)	overloading for Unary operator.	7M									
	b)	Define Polymorphism. How virtual function avoids ambiguity in multipath inheritance. <b>OR</b>	7M									
4.	a)	Compare Time and Space complexity. Explain with suitable examples.	7M									
4.			7M									
<ul> <li>b) Demonstrate an abstract class with a suitable C++ program.</li> <li>UNIT-III</li> </ul>												
5.	a)	Demonstrate ADT implementation of Stack using C++ program.	9M									
	b)	Define Hashing. Explain about hash functions.	5M									
		OR										
6.	a)	Explain the operations performed on Linear list with suitable examples.	8M									
	b)	Compare Double Hashing and Extendable Hashing.										
		UNIT–IV										
7.	a)	Define BST. Demonstrate its operations with suitable examples.	7M									
	b)	Demonstrate Binary Tree Traversal Techniques with algorithms.	7M									
		OR										
8.	a)	Demonstrate Priority Queue implementation using Heaps.	7M									
	b)	Define AVL Tree. Demonstrate its operations with suitable examples	7M									
0		UNIT-V Demonstrate insertion and deletion energians in P. Tree with example	014									
9.	a) b)	Demonstrate insertion and deletion operations in B-Tree with example.	8M 6M									
	b)	What is a Red-Black Tree? List its properties. <b>OR</b>	6M									
10.	a)		9M									
	b)	Create a Red-Black Tree by inserting the following sequence of numbers:										
		8, 18, 5, 15, 17, 25, 40 and 80.	5M									
		***										

Hall	Tick	et Number :										<b></b>		
Code	<b>: 7</b> G	132	I	I	<u>.t</u>	1	ı <u> </u>	I	<u>I</u>			R-	17	
		II B.Tech. I S	Seme	ster Su	Jpp	leme	entary	Exar	minat	ions	s May	/ 2019		
							geme		-					
Max	Mc	arks: 70	(Cor	npute	er Sc	ienc	e and I	ngir	neering	g)		Time:	3 Ног	irs
		ver all five unit	s by cł	noosin	g on		estion fr	om e	ach u	nit (	5 x 14			
							UNIT-I							
1.	a)	List and expl	ain the	disad	vanta	iges	of file pr	ocess	sing sy	rsterr	าร.			10M
	b)	Write about i	nstanc	es and	sch	emas								4M
0	<b>OR</b> 2 a) Write short notes on data manipulation language and data definition language													
<ol> <li>a) Write short notes on data manipulation language and data definition language for relational databases.</li> </ol>											10M			
	b)	Write about t			of da	tabas	se admi	nistra	tor.					4M
	,													
	,			=			UNIT-II				•.			
3.	a)	What is an E attributes.	-R mo	del? E	xplair	n with	i suitabl	e exa	mples	, ent	ity, en	tity sets,	and	7M
	b)	What is aggr	egation	n in E-l	R mo	del?	Explain	it witl	h an e>	kamr	ole.			7M
	,		- 3				OR							
4.		Explain logic	al data	base c	lesig	n: EF	to Rela	tiona	d.					14M
							UNIT–II	I						
5.	a)	Briefly discus	ss abou	ut data	defir	nition			n SQL.					7M
	b)	Write short n									QL.			7M
							OR							
6.	a)	Briefly discus	ss abou	ut SQL	join	oper	ators wit	h exa	amples	5.				7M
	b)	Write short n	otes or	n trigge	ers.									7M
							UNIT-IV	1						
7.	a)	What is norm	nal forn	ר? Exp	lain v				and B	BCNF	=.			10M
	b)	Write about t	he pro	blems	relate	ed de	compos	sition.						4M
							OR							
8.	a)	Briefly discus			-		•				•			7M
	b)	Illustrate mul	tivalue	d depe	ender	ncies	and fou	rth no	ormal f	orm	with e	xample.		7M
							UNIT-V	'						
9.	a)	What is trans	saction	? List a	and e	xplai			ies of t	rans	action			7M
	b)	Write motiva					executio	on of	f trans	sactio	ons. I	Explain	with	
		example, ser	rializab	le sche	edule									7M
40	- )	Evelate to 1					OR							714
10.	a) b)	Explain in de												7М 7М
	b)	Write short n	ULES OI		ees.	*	**							7M

										]			l		
Hall	Tick	et Number :												D 17	
Code	<b>e: 7</b> G	134												R-17	
		ll B.Tech. I	Sem						-			tion	s May	y 2019	
			10				-	-	-	<b>atic</b> : ngin	-				
Мах	. Mo	arks: 70		2011	pule	51 30		.e ui		ngin	CCIII	ig j		Time: 3 Ho	Urs
ŀ	۹nsw	er all five uni	its by	chc	osinę	g on		estio *****	n fro	m eo	ach i	unit (	5 x 14	= 70 Marks )	
								JNIT	-1						
1.	a)	show that ]	( <i>P</i> ∧	Q) -	→ (ヿ I	Pv(		_		P	(Q)				7N
	b)	show that (													
	0)	Show that (	100	( Y	AR)	) v (	Q //I				'n				7N
0	、							OF		<b>6</b> 41					
2.	a)	Obtain the p $(\exists P \rightarrow R) \land$	-		onjur	nctive	e nor	malf	orm	of the	e sta	teme	ent		7N
	b)				olid o	anal	unior	of t		omio	(I	nun	) (n	$\mathbf{D}(0 \times \mathbf{C})$	7 10
	D)	using rules of				Onci	u5101		ie pi	enns	62 (1	νų	), (F -	$\rightarrow R$ ), $(Q \rightarrow S)$	7N
		5					ι	JNIT-	-11						
3.	a)	Define the fo	ollowi	ing a	ind g	ive s				les fo	or ea	ch			
		i. Lattice													
	ii. Sub lattice														
		iii. Complem						_							6N
	b)	Let n be a p			-										
		the relation and 30.	ot "di	VISIO	n". D	raw	the a	lagra	ams	or lat	lices	() <sub>21</sub> ,L	J) for r	1=6,8, 24	8N
		anu su.						OF	,						OIV
4.	a)	Civo an oxa	mnlo	ofa	rolat	lion	which			otrio	anti	ev mer	notrio	compatibility	
4.	a)	and transitiv	•	UI a	Tela		WINCI	113 3	yııııı	enic,	anu	Synn	neine,	compationity	7N
	b)	Let Z={-2,-1	,0,1,2	2,3,	} a	nd R	elatio	on R	is de	efined	d as				
		R={(x,y)/x-y	is div	/isibl	e by	3} fir	nd the	e rela	ation	s on	Z.				7N
							U	INIT-	-111						
5.	a)	Let ({a,b},*)	be a	sem	i gro	up w	here	a*a=	b sh	ow th	nat i)	a*b=	⊧b*a ii	) b*b=a.	7N
	b)	Show that e	very	cycli	c gro	up is	abe	lian g	group	Э.					7N
								OF	ł						
6.	a)	How many a least one sid		-			here	of th	e sei	{8a,6	6b,7c	:} in v	which '	a' is an at	7N
	b)	Prove by pig were born in	-		•	•	that	in a (	group	o of 6	61 pe	ople,	, at lea	st 6 people	7N

7M

7M

7M

	UNIT–IV	
--	---------	--

7.	a)	Find the coefficient of $x^{18}$ in the following product	
		$(x+x^2+x^3+x^4+x^5) (x^2+x^3+x^4+)^5$	7M
	b)	Find a generating function for the recurrence relation	
		$a_{n+2}$ – $5a_{n+1}$ + $6a_n$ = 2 where n 0 and $a_0$ = 3, $a_1$ = 7. Hence solve the relation.	7M

OR

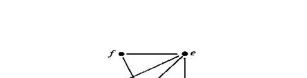
- 8. a) Solve the Recurrence Relation  $a_n 7a_{n-1} + 10a_{n-2} = 0$  where  $a_0 = 1$  and  $a_1 = 41$ . 7M
  - b) Solve the Recurrence Relation  $a_n 6a_{n-1} + 8a_{n-2} = 3^n$  where  $a_0 = 3$  and  $a_1 = 7$ . 7M

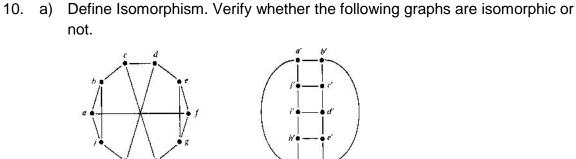
#### UNIT–V

Explain the DFS algorithm. Using DFS find the spanning tree of the following

OR

9. a) Define chromatic number. Find the chromatic number of the following graph.

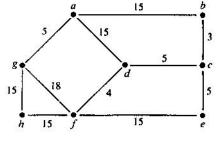




b)

graph.

b) Illustrate Prim's algorithm to find a minimal spanning tree for the weighted graph given below.





7M



b) i) Perform the subtraction in Excess-3 code using the 10's complement method: 597-239. ii) State De Morgan's theorem for three variables 7M <b>OR</b> 2. a) i) Prove that $(\overline{A + BC}) (A\overline{B} + A\overline{BC}) = \overline{ABC}$ . ii) Implement OR Gate using NAND Gates 7M b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M <b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) 10M b) Show that the dual of the exclusive-OR is equal to its complement 4M <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M <b>UNIT-III</b> 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M c) <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
II B.Tech. I Semester Supplementary Examinations May 2019 Digital Logic Design ( Computer Science and Engineering ) Max. Marks: 70 Answer all five units by choosing one question from each unit ( $5 \times 14 = 70$ Marks) ************************************																								
(Computer Science and Engineering )Time: 3 HoursAnswer all five units by choosing one question from each unit ( $5 \times 14 = 70$ Marks )***********************************																								
Max. Marks: 70 Answer all five units by choosing one question from each unit ( $5 \times 14 = 70$ Marks) <b>UNIT-1</b> 1. a) i) Convert (4057.06) <sub>8</sub> to binary code. ii) What is reflection code? Give Example b) i) Perform the subtraction in Excess-3 code using the 10's complement method: $597-239$ . ii) State De Morgan's theorem for three variables <b>OR</b> 2. a) i) Prove that $(\overline{A + BC}) (A\overline{B} + \overline{ABC}) = \overline{ABC}$ . ii) Implement OR Gate using NAND Gates b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M <b>UNIT-11</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) b) Show that the dual of the exclusive-OR is equal to its complement <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. M b) Minimize the function f = $\Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it <b>UNIT-11</b> 5. a) Design 4-bit binary to Gray code converter. b) Implement the function f(A,B,C)= $\Sigma m(0.2,5,7)$ using 4×11 MUX. <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. <b>F</b> (W <b>VIIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. <b>F</b> (A) What is difference between latch and flip flop? Explain about clocked RS flip																								
Answer all five units by choosing one question from each unit ( $5 \times 14 = 70$ Marks) <b>UNIT-I</b> 1. a) i) Convert (4057.06) <sub>8</sub> to binary code. ii) What is reflection code? Give Example 7M b) i) Perform the subtraction in Excess-3 code using the 10's complement method: $597-239$ . ii) State De Morgan's theorem for three variables 7M <b>OR</b> 2. a) i) Prove that $(\overline{A + BC}) (A\overline{B} + \overline{ABC}) = \overline{ABC}$ . ii) Implement OR Gate using NAND Gates 7M b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M <b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) 10M b) Show that the dual of the exclusive-OR is equal to its complement 4M <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M <b>UNIT-II</b> 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
$\begin{tabular}{ c c c c c } \hline UNIT-I \\ 1. a) i) Convert (4057.06)_6 to binary code. \\ ii) What is reflection code? Give Example 7M \\ b) i) Perform the subtraction in Excess-3 code using the 10's complement method: 597-239. \\ ii) State De Morgan's theorem for three variables 7M \\ \hline OR 7M \\ \hline O$																								
1. a) i) Convert (4057.06) <sub>8</sub> to binary code. ii) What is reflection code? Give Example 7M b) i) Perform the subtraction in Excess-3 code using the 10's complement method: 597-239. ii) State De Morgan's theorem for three variables 7M <b>OR</b> 2. a) i) Prove that $\overline{(A + BC)} (AB + ABC) = ABC.$ ii) Implement OR Gate using NAND Gates 7M b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M <b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) 10M b) Show that the dual of the exclusive-OR is equal to its complement 4M <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M b) Minimize the function $f(A, B, C) = \Sigma m(0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$ using K-Map and obtain SOP form of it 7M <b>UNIT-III</b> 5. a) Design 4-bit binary to Gray code converter. b) Implement the function $f(A, B, C) = \Sigma m(0, 2, 5, 7)$ using 4x1 MUX. <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. b) Realize the function $\Sigma m(0, 3, 5, 6, 7)$ using 8:1 multiplexer 7M <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
ii)What is reflection code? Give Example7Mb)i)Perform the subtraction in Excess-3 code using the 10's complement method: 597-239.7Mii)State De Morgan's theorem for three variables7MOR2a)i)Prove that $(\overline{A + BC}) (A\overline{B} + \overline{ABC}) = \overline{ABC}$ . ii)7MImplement OR Gate using NAND Gates7Mb)i)Perform subtraction using 2's complement: 1100010 - 11001117MImplement OR Gate using NAND Gates7Mii)Perform subtraction using 2's complement: 1100010 - 11001117MImplement OR Gate using complement: 1100010 - 1100111Implement OR Gate using 2's complement: 1100010 - 1100111Implement OR Gate using 2's complement: 1100010 - 1100111Implement ORImplement OR Gate using 2's complement: 1100010 - 1100111Implement OR Gate using 2's complement: 1100010 - 1100111Implement: Implement ORImplement: Implement ORORImplement Or Gate colspan="2">Implement ORImplement ORImplement ORImplement ORImplement ORImplement ORImplement of Implement DevelopmentORImplement ORImplement of Implement DevelopmentImplement of Implement Part Pa																								
method: 597-239. ii) State De Morgan's theorem for three variables OR OR 2. a) i) Prove that $(\overline{A + BC}) (A\overline{B} + A\overline{BC}) = \overline{ABC}$ . ii) Implement OR Gate using NAND Gates 7M b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M UNIT-II 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) 10M b) Show that the dual of the exclusive-OR is equal to its complement 4M OR 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M UNIT-III 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. 7M OR 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M CUNIT-IV 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
ii) State De Morgan's theorem for three variables $OR$ OR 2. a) i) Prove that $(\overline{A + BC}) (A\overline{B} + \overline{ABC}) = \overline{ABC}$ . ii) Implement OR Gate using NAND Gates 7M b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M <b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) 10M b) Show that the dual of the exclusive-OR is equal to its complement 4M <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it <b>UNIT-II</b> 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
OR2. a) i) Prove that $(\overline{A + BC}) (A\overline{B} + \overline{ABC}) = \overline{ABC}$ . ii) Implement OR Gate using NAND Gates7Mb) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 11001117M <b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13)10MOR4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ.7M <b>OR</b> 4. a) Design 4-bit binary to Gray code converter.MINIT-III5. a) Design 4-bit binary to Gray code converter.OR6. a) Implement a full-adder circuit with a decoder and two OR gates.7M <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.ON What is difference between latch and flip flop? Explain about clocked RS flip																								
ii) Implement OR Gate using NAND Gates 7M b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M <b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) 10M b) Show that the dual of the exclusive-OR is equal to its complement 4M <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \sum m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M <b>UNIT-III</b> 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \sum m(0,2,5,7)$ using 4x1 MUX. 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\sum m(0,3,5,6,7)$ using 8:1 multiplexer 7M 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
ii) Implement OR Gate using NAND Gates 7M b) i) Reduce the following Boolean expression to 3 literals. [CD' +A]'+ A+CD+AB ii) Perform subtraction using 2's complement: 1100010 - 1100111 7M <b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13) 10M b) Show that the dual of the exclusive-OR is equal to its complement 4M <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \sum m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M <b>UNIT-III</b> 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \sum m(0,2,5,7)$ using 4x1 MUX. 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\sum m(0,3,5,6,7)$ using 8:1 multiplexer 7M 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
ii) Perform subtraction using 2's complement: 1100010 - 11001117MUNIT-IIUNIT-II3. a) Simplify the following expression into sum of products using Karnaugh map: $F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13)$ 10Mb) Show that the dual of the exclusive-OR is equal to its complement4MOR0R4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: $F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ.$ 7Mb) Minimize the function $f = \Sigma m(0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$ using K-Map and obtain SOP form of it7M5. a) Design 4-bit binary to Gray code converter. b) Implement the function $f(A, B, C) = \Sigma m(0, 2, 5, 7)$ using 4x1 MUX. OR7M6. a) Implement a full-adder circuit with a decoder and two OR gates.7Mb) Realize the function $\Sigma m(0, 3, 5, 6, 7)$ using 8:1 multiplexer7M7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.7Mb) What is difference between latch and flip flop? Explain about clocked RS flip																								
<b>UNIT-II</b> 3. a) Simplify the following expression into sum of products using Karnaugh map: $F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13)$ 10Mb) Show that the dual of the exclusive-OR is equal to its complement4M <b>OR</b> 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: $F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ.$ b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it7M <b>UNIT-III</b> 5. a) Design 4-bit binary to Gray code converter. b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. <b>OR</b> 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer7M <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.7M <b>What</b> is difference between latch and flip flop? Explain about clocked RS flip																								
3. a) Simplify the following expression into sum of products using Karnaugh map: $F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13)$ 10M         b) Show that the dual of the exclusive-OR is equal to its complement       4M         OR         4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: $F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ.       7M         b) Minimize the function f = \Sigma m(0,2,4,6,7,8,10,12,13,15) using K-Map and obtain SOP form of it       7M         Solution of the function f = \Sigma m(0,2,4,6,7,8,10,12,13,15) using K-Map and obtain SOP form of it         OR         6. a) Design 4-bit binary to Gray code converter.         b) Implement a full-adder circuit with a decoder and two OR gates.         MINIT-IV         7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.         The What is difference between latch and flip flop? Explain about clocked RS flip   $																								
F(A, B, C, D) = $(1, 3, 4, 5, 6, 7, 9, 12, 13)$ 10Mb) Show that the dual of the exclusive-OR is equal to its complement4MOR4.a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WYY + WYZ + WYZ.7Mb) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it7M <b>UNIT-III</b> 7.a) Design 4-bit binary to Gray code converter. Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. OR7M6.a) Implement a full-adder circuit with a decoder and two OR gates.7M <b>b</b> ) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer7M <b>7.</b> a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.7Mb) What is difference between latch and flip flop? Explain about clocked RS flip7M																								
b) Show that the dual of the exclusive-OR is equal to its complement $OR$ 4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: F(W, X, Y, Z) = XZ + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M <b>UNIT-III</b> 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
OR4. a) Simplify the following Boolean expressions using K-map and implement them using NAND gates: $F(W, X, Y, Z) = XZ + WXY + WYZ + WYZ. WYZ. 7M$ b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M7MUNIT-III5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. 7M Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7MUNIT-IV7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7Mb) What is difference between latch and flip flop? Explain about clocked RS flip																								
using NAND gates: F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ. 7M b) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M <b>UNIT-III</b> 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. 7M <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer 7M <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip																								
F(W, X, Y, Z) = XZ + WXY + WXY + WYZ + WYZ.7Mb) Minimize the function $f = \Sigma m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it7MUNIT–III5. a) Design 4-bit binary to Gray code converter.7Mb) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX.7MOR6. a) Implement a full-adder circuit with a decoder and two OR gates.7MDesign 4-bit binary to Gray code converter.7MOR6. a) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX.7MOR <tr <td="" colspan="&lt;/td"></tr> <tr><td>b) Minimize the function <math>f = \sum m(0,2,4,6,7,8,10,12,13,15)</math> using K-Map and obtain SOP form of it 7M UNIT-III 5. a) Design 4-bit binary to Gray code converter. 7M b) Implement the function <math>f(A,B,C) = \sum m(0,2,5,7)</math> using 4x1 MUX. 7M OR 6. a) Implement a full-adder circuit with a decoder and two OR gates. 7M b) Realize the function <math>\sum m(0,3,5,6,7)</math> using 8:1 multiplexer 7M UNIT-IV 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M b) What is difference between latch and flip flop? Explain about clocked RS flip</br></td></tr> <tr><td>SOP form of it       7M         UNIT-III       0         5. a) Design 4-bit binary to Gray code converter.       7M         b) Implement the function <math>f(A,B,C) = \Sigma m(0,2,5,7)</math> using 4x1 MUX.       7M         OR       0         6. a) Implement a full-adder circuit with a decoder and two OR gates.       7M         b) Realize the function <math>\Sigma m(0,3,5,6,7)</math> using 8:1 multiplexer       7M         UNIT-IV       7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M</td></tr> <tr><td>5. a)Design 4-bit binary to Gray code converter.7Mb)Implement the function <math>f(A,B,C) = \Sigma m(0,2,5,7)</math> using 4x1 MUX.7MOR6. a)Implement a full-adder circuit with a decoder and two OR gates.7Mb)Realize the function <math>\Sigma m(0,3,5,6,7)</math> using 8:1 multiplexer7MUNIT-IV7. a)With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.7Mb)What is difference between latch and flip flop? Explain about clocked RS flip7M</td></tr> <tr><td>b) Implement the function <math>f(A,B,C) = \Sigma m(0,2,5,7)</math> using 4x1 MUX. <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. b) Realize the function <math>\Sigma m(0,3,5,6,7)</math> using 8:1 multiplexer <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. b) What is difference between latch and flip flop? Explain about clocked RS flip</td></tr> <tr><td>OR         6. a) Implement a full-adder circuit with a decoder and two OR gates.       7M         b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer       7M         UNIT–IV         7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M</td></tr> <tr><td><ul> <li>6. a) Implement a full-adder circuit with a decoder and two OR gates.</li> <li>b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer</li> <li>7M</li> <li>UNIT-IV</li> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul></td></tr> <tr><td><ul> <li>b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer 7M</li> <li>UNIT-IV</li> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul></td></tr> <tr><td>UNIT-IV         7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M</td></tr> <tr><td><ul> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul></td></tr> <tr><td>b) What is difference between latch and flip flop? Explain about clocked RS flip</td></tr> <tr><td></td></tr> <tr><td>TIOP USING NAND gates /M</td></tr> <tr><td>OR</td></tr> <tr><td>8. a) With a neat diagram, explain master slave JK Flip Flop 7M</td></tr> <tr><td>b) Explain the operation of universal shift register. 7M</td></tr> <tr><td>UNIT-V</td></tr> <tr><td>9. a) Draw and explain the operation of 4 bit ring counter. 7M</td></tr> <tr><td><ul><li>b) i) Compare PLA with PROM.</li><li>ii) What is ROM? List the different types of ROMs 7M</li></ul></td></tr> <tr><td>OR</td></tr> <tr><td>10. a) Draw and explain 4-bit Johnson counter using D-flip flop.7M</td></tr> <tr><td>b) Implement the following functions using PLA.</td></tr> <tr><td>A (x,y,z) = m (1,2,4,6) B (x,y,z) = m (0,1,6,7)</td></tr> <tr><td>B(x,y,z) = m(0,1,6,7)</td></tr> <tr><td>C(x,y,z) = m(2,6) 7M</td></tr>	b) Minimize the function $f = \sum m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M UNIT-III 	SOP form of it       7M         UNIT-III       0         5. a) Design 4-bit binary to Gray code converter.       7M         b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX.       7M         OR       0         6. a) Implement a full-adder circuit with a decoder and two OR gates.       7M         b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer       7M         UNIT-IV       7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M	5. a)Design 4-bit binary to Gray code converter.7Mb)Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX.7MOR6. a)Implement a full-adder circuit with a decoder and two OR gates.7Mb)Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer7MUNIT-IV7. a)With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.7Mb)What is difference between latch and flip flop? Explain about clocked RS flip7M	b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. b) What is difference between latch and flip flop? Explain about clocked RS flip	OR         6. a) Implement a full-adder circuit with a decoder and two OR gates.       7M         b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer       7M         UNIT–IV         7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M	<ul> <li>6. a) Implement a full-adder circuit with a decoder and two OR gates.</li> <li>b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer</li> <li>7M</li> <li>UNIT-IV</li> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul>	<ul> <li>b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer 7M</li> <li>UNIT-IV</li> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul>	UNIT-IV         7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M	<ul> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul>	b) What is difference between latch and flip flop? Explain about clocked RS flip		TIOP USING NAND gates /M	OR	8. a) With a neat diagram, explain master slave JK Flip Flop 7M	b) Explain the operation of universal shift register. 7M	UNIT-V	9. a) Draw and explain the operation of 4 bit ring counter. 7M	<ul><li>b) i) Compare PLA with PROM.</li><li>ii) What is ROM? List the different types of ROMs 7M</li></ul>	OR	10. a) Draw and explain 4-bit Johnson counter using D-flip flop.7M	b) Implement the following functions using PLA.	A (x,y,z) = m (1,2,4,6) B (x,y,z) = m (0,1,6,7)	B(x,y,z) = m(0,1,6,7)	C(x,y,z) = m(2,6) 7M
b) Minimize the function $f = \sum m(0,2,4,6,7,8,10,12,13,15)$ using K-Map and obtain SOP form of it 7M UNIT-III 																								
SOP form of it       7M         UNIT-III       0         5. a) Design 4-bit binary to Gray code converter.       7M         b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX.       7M         OR       0         6. a) Implement a full-adder circuit with a decoder and two OR gates.       7M         b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer       7M         UNIT-IV       7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M																								
5. a)Design 4-bit binary to Gray code converter.7Mb)Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX.7MOR6. a)Implement a full-adder circuit with a decoder and two OR gates.7Mb)Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer7MUNIT-IV7. a)With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.7Mb)What is difference between latch and flip flop? Explain about clocked RS flip7M																								
b) Implement the function $f(A,B,C) = \Sigma m(0,2,5,7)$ using 4x1 MUX. <b>OR</b> 6. a) Implement a full-adder circuit with a decoder and two OR gates. b) Realize the function $\Sigma m(0,3,5,6,7)$ using 8:1 multiplexer <b>UNIT-IV</b> 7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. b) What is difference between latch and flip flop? Explain about clocked RS flip																								
OR         6. a) Implement a full-adder circuit with a decoder and two OR gates.       7M         b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer       7M         UNIT–IV         7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M																								
<ul> <li>6. a) Implement a full-adder circuit with a decoder and two OR gates.</li> <li>b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer</li> <li>7M</li> <li>UNIT-IV</li> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul>																								
<ul> <li>b) Realize the function Σm(0,3,5,6,7) using 8:1 multiplexer 7M</li> <li>UNIT-IV</li> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop. 7M</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul>																								
UNIT-IV         7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.       7M         b) What is difference between latch and flip flop? Explain about clocked RS flip       7M																								
<ul> <li>7. a) With the help of conversion table, K-map and the logic diagram explain the steps used to convert a J-K flip-flop to a D flip-flop.</li> <li>b) What is difference between latch and flip flop? Explain about clocked RS flip</li> </ul>																								
b) What is difference between latch and flip flop? Explain about clocked RS flip																								
TIOP USING NAND gates /M																								
OR																								
8. a) With a neat diagram, explain master slave JK Flip Flop 7M																								
b) Explain the operation of universal shift register. 7M																								
UNIT-V																								
9. a) Draw and explain the operation of 4 bit ring counter. 7M																								
<ul><li>b) i) Compare PLA with PROM.</li><li>ii) What is ROM? List the different types of ROMs 7M</li></ul>																								
OR																								
10. a) Draw and explain 4-bit Johnson counter using D-flip flop.7M																								
b) Implement the following functions using PLA.																								
A (x,y,z) = m (1,2,4,6) B (x,y,z) = m (0,1,6,7)																								
B(x,y,z) = m(0,1,6,7)																								
C(x,y,z) = m(2,6) 7M																								

		(	Comr	outer Scienc	Se and End	•							
Ма	x. M	ہ arks: 70	Comp			Jineening j	Time: 3 H	ours					
		wer all five units l	by cho	osing one qu	*****	n each unit ( 5 :							
					UNIT–I								
1.	a)	List and explain	the attr	ibutes of <body></body>	ody> tag and	d <frame/> tag.		10M					
	b)	List and explain	the imp	oortant applic	ations of inf	ernet in brief.		4M					
					OR								
2.	a)	How to create lis an example.	sts in H <sup>-</sup>	TML? What a	are the differ	ent types of Lis	ts? Explain with	10M					
	b)	Write a HTML c	ode to r	navigate betv	veen two we	eb pages using	<a href=""> tag.</a>	4M					
		UNIT–II											
3.		Write a HTML code to create a BIODATA form for displaying the user details. Name, Phone Number should be accepted as a Textbox, address should be accepted as a Textarea. For gender use Radio Button and for hobbies (Reading, Cooking, Watching TV, Playing) use check Box. 14M											
					OR								
4.	. Write a HTML code to create the following table using HTML  elements and attributes.												
			S.No	Reg. No.	Branch	Percentage							
		-	1	BCE001	005	72%							
			2	BCE002	CSE	75%							
		-	3	BEE015	505	700/							
		-	4	BEE006	ECE	73%		14M					
		L			UNIT–III								
5.	a) b)	<last:  <email>alee <phone>123 <birthday> <year< td=""><td>= "1.0" &gt;Alice &gt;Lee (@aol.c -45-67 -45-67 </td><td>or the follow ?&gt; c/first&gt; ast&gt; om</td></year<></birthday></phone></email> 89 c/year&gt; c/year&gt;</last: 	= "1.0" >Alice >Lee (@aol.c -45-67 -45-67 	or the follow ?> c/first> ast> om	ing xml do	cument		10M 4M					
					OR								
							Page	e <b>1</b> of <b>2</b>					

### Code: 7G135

II B.Tech. I Semester Supplementary Examinations May 2019

## Web Programming

- 3
- 4

		Code: 7G	Code: 7G135	
6.	a)	With an example, describe CSS style properties associated with text formatting.	7M	
	b)	With an example, describe CSS style properties associated with BOX model.	7M	
		UNIT-IV		
7.	a)	What are the merits and de-merits of client side scripting	4M	
	b)	Write a javascript program that displays "Good Morning", or "Good Afternoon" or "Good Evening" based on the time extracted from the Date().	10M	
OR				
8.		Create an online application form and validate the fields email_id and phone number using javascript program.	14M	
		UNIT-V		
9.	a)	Explain the role of jQuery.	4M	
	b)	Write a jQuery code to apply the two different colors on alternate rows in a table.	10M	
OR				
10.		Name any five jQuery Events. Illustrate the usage of those events with an example.	14M	