Code : 1PC326

R-11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech II Semester Regular December, 2013

Hardware Description Languages
(ES)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1.	a.	List out the various Data types that are used in Verilog HDL. Explain them in detail. What the logic levels are used in Verilog HDL.	**8M**
	b.	With an example explain the structure of module.	**4M**
2.	a.	Describe Delay Back Annotation, Draw the flow diagram of delay back annotation.	**7M**
	b.	Write about path delays.	**5M**
3.	a.	With a neat sketch describe the Moore Machine .	**4M**
	b.	Draw the state diagram of Melay Machine, and write a Verilog code in Behavioral description.	**8M**
4.	a.	With a neat sketch describe the logic synthesis flow.	**5M**
	b.	Draw the diagram of 4X1 multiplexer using logic gates and write a Verilog code in Dataflow description.	**7M**
5.	a.	Explain the conditional statements, multiway branching statements, looping statements with an example.	**6M**
	b.	Describe the Parallel blocks ,Sequential blocks with an example.	**6M**
6.	a.	Describe the strength levels in Verilog. What is meant by Contention? When contention arises how it can be resolve using strength levels.	**7M**
	b.	Write a Verilog Code for CMOS NOR gate with delay values in Switch level modeling.	**5M**
7.	a.	Explain the Top-Down and Bottom -Up design methodology.	**6M**
	b.	Describe the various VHDL Operators.	**6M**
8.	a.	Write about Assertion statement in VHDL with syntax.	**6M**
	b.	Write a VHDL code for D-Flip Flop in Behavioral description.	**6M**

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech II Semester Regular December, 2013
Hardware Software Co –Design
(*Common ES & VLSI Sys D*)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* full questions
All Questions carry equal marks (12 Marks each)

1.	a.	Explain the architectures related to Co-Design issues.	6 M
	b.	State and explain various Co-Design languages.	6 M
2.	a.	List and explain any two hardware structure synthesis algorithms.	8 M
	b.	Describe the distributed system Co-Synthesis	4 M
3.	a.	Differentiate Prototyping and Emulation techniques.	6 M
	b.	Discuss about Prototyping and Emulation environments.	6 M
4.	a.	What is a Mixed System? Enumerate with the help of an example.	8 M
	b.	Explain the architecture for data dominated systems.	4 M
5.		With the help of a diagram explain modern Embedded architecture and discuss about their compilation techniques.	12 M
6.	a.	Write brief notes on Design Verification.	6 M
	b.	Distinguish between design Specification and Verification.	6 M
7.		Describe various system level specification languages.	12 M
8.	a.	Explain What is Heterogeneous Specification?	6 M
	b.	Write about partitioning sessions in Lycos.	6 M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. II Semester Regular Examinations, December 2013
Radio Frequency Identification
(ES)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1.	a.	What are the advantages of automatic Identification system? Explain how a biometric procedures system works?	6M
	b.	Explain briefly the different components of RFID system?	6M
2.	a.	Write briefly about the fundamental differential features.	5M
	b.	"Selection criteria for RFID system is critical". Justify?	7M
3.	a.	Write about Inductive coupling with neat diagram in HDX/FDX and SEQ systems.	8M
	b.	Discuss briefly about 1-bit transponder.	4M
4.	a.	Explain about Microprocessors dual interface card.	7M
	b.	Explain about measurement of physical variables using microwave transponders.	5M
5.		Explain Total Transponder – reader system	12M
6.	a.	Explain about any two Digital modulation procedures.	8M
	b.	Write in detail about modulation procedures with subcarrier	4M
7.	a.	Write about FDMA and Binary search algorithm procedure.	6M
	b.	Why Data security is important? Explain about Encrypted data transfer?	6M
8.	a.	Write short notes on ExxonMobil Speed pass?	4M
	b.	Write short notes on (i)NFC applications and (ii) Contactless Smart cards	8M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

M.Tech. II Semester Regular Examinations, December 2013

Testing and Testability

(*Common ES & VLSI Sys D*)

Max. Marks: 60 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (12 Marks each)

1.	a.	With examples discuss about gate level event driven simulation.	06M
	b.	Discuss about delay models with examples.	06M
2.	a.	Construct a circuit that has two independent faults.	04M
	b.	List out the limitations of parallel fault simulation.	04M
	c.	Distinguish between single stuck and multiple stuck at faults.	04M
3.	a.	Explain about automated test pattern generation for detecting SSF's in combinational circuits.	06M
	b.	Discuss about ATPG vectors, formats, compaction and compression.	06M
4.	a.	Discuss about Boundary Scan Standards and Compression Techniques.	06M
	b.	Explain about generic boundary scan and full serial integrated scan.	06M
5.	a.	Give a detail view on syndrome test with examples.	06M
	b.	With neat diagrams discuss about Controllability and Observability.	06M
6.	a.	Discuss briefly about the following BIST Architectures. (i) STUMPS (ii) CBIST (iii) CEBS (iv) RTD	08M
	b.	Discuss about the need for Test Pattern Generation with examples.	04M
7.	a.	Discuss about Memory Test Architectures and Techniques.	06M
	b.	Discuss about Types of Memories and Integration.	06M
8.		Discuss in detail about JTAG Testing Features.	12M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech II Semester Regular December, 2013

DSP Processors and Architectures
(Common to DECS, ES & VLSI Sys D)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a. What are the various types of elementary sequences in digital signal processing for analysis purpose? Give their definition and MATLAB representations? 6M
   b. Explain the digital fitters with neat sketches. 6M
2. a. Explain briefly DSP computational errors. 6M
   b. Explain with suitable example the analysis of D/A conversion errors using MATLAB. 6M
3. Explain briefly the DSP computational building blocks with suitable architecture. 12M
4. Explain the following terms: 12M
   i) Pipeline depth
   ii) Branching effect.
   iii) Interrupt effects.
   iv) Stacks
5. a. Explain the memory organization in TMS 320C54XX DSP . 6M
   b. Explain the operation of parallel instruction of TMS 320C54XX. 6M
6. a. Write an algorithm to implement the FIR filter. 6M
   b. Explain how an adaptive filter can be implemented using LMS algorithms. 6M
7. a. Write an algorithm to implement an 8 point (DIT-FFT) on TMS 320C54XX. 6M
   b. Explain the computation of the signal spectrum and how it can be implemented on DSP. 6M
8. a. Explain how DMA is interfaced to a DSP. 6M
   b. Draw the CODEC interface circuit and explain. 6M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech II Semester Regular December, 2013
Embedded Software Design
(*ES*)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1.	a.	Explain super scalar architecture used in Pentium processor?	6M
	b.	Discuss functions of special registers in Pentium micro processor?	6M
2.		Explain an embedded design life cycle diagram? Discuss briefly about different phases represented in design life cycle diagram?	12M
3.	a.	Write note on debugging of an embedded system design?	6M
	b.	What are the significant issues considered while choosing Micro processor?	6M
4.		Explain in detail about special software techniques used in an embedded design?	12M
5.	a.	Write note on back ground debug mode. Mention its advantages and disadvantages?	6M
	b.	Explain the use and significance of JTAG and Nexus in Embedded firmware?	6M
6.	a.	Write note on hardware and software instrumentation used in testing?	6M
	b.	Write note on maintenance and testing?	6M
7.		Explain compilation process with help of block diagram?	12M
8.	a.	Write note on memory leakage?	6M
	b.	What are buffer over-run and buffer under-run states? Explain the reasons for their occurrence?	6M

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