Code : 1PB323 **R11**

M.Tech. II Semester Regular Examinations, July/August 2014

DSP PROCESSORS AND ARCHITECTURES

(Common to Embedded Systems & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Draw the block diagram of DSP systems and write advantages & disadvantages? 6M
   b) Find the convolution of given sequences:
   $x_1(n) = \{3, 4.2, 11, 0, 7, -1, 0, 2\}$, n=0.....7
   $x_2(n) = \{1.2, 3, 0, -0.5.2\}$, n=0.....4 6M
2. a) Explain about fixed point and floating point format representations with an example. 6M
   b) Compare the dynamic range and percentage resolution of a signal that uses:
      i. 16-point fixed point format.
      ii. 32-point floating point format with 14 bit for the mantissa and 8- bit for the exponent. 6M
3. a) Explain the structure of 4 × 4 Broun multiplier. 6M
   b) Write about Data addressing capabilities and explain special addressing modes. 6M
4. a) Explain the following terms in Pipelining:
      i. Interlocking.
      ii. Branching effect. 6M
   b) Distinguish between maskable and non maskable, software and hardware interrupts. 6M
5. a) What are the architectural features of 54XX processor? Explain with a block diagram. 6M
   b) What are various interrupts of 54XX DSP Processors? 6M
6. a) Represent each of the following as 16-bit numbers in the desired Q-notation:
      i) 0.3125 as Q15 number.
      ii) -0.3125 as Q15 number.
      iii) 3.125 as a Q7 number.
      iv) -352 as Q0 number. 6M
   b) Write a program to multiply a Q15 number with a Q15 number to obtain the result in Q15 notation. 6M
7. a) Explain how overflow conditions be avoided by scaling the numbers in FFT computation. 6M
   b) Explain the procedure to generate bit-reversed index for 4-bit and show the result for all possible combinations. 6M
8. a) Draw the memory map representation of TMS 5416 DSP and explain clearly. 6M
   b) Write notes on MCBSPS. 6M

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M.Tech. II Semester Regular Examinations, July/August 2014

EMBEDDED SOFTWARE DESIGN

(Embedded Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	With a neat sketch explain about Pentium microprocessor organization?	6M
	b)	Explain about Pentium memory management?	6M
2.		Explain in detail embedded design life cycle, and explain hardware/ software integration?	12M
3.		Write short notes on the following (a) Hardware/Software partitioning (b) Hardware/Software duality. (c) BDM.	12M
4.		Detail the use of Buffering and explain its other DATA structures?	12M
5.		Write briefly about the following. (a) selection process (b) hardware trends	12M
6.	a)	What is Flash memory? Explain about various design methodologies of flash memory?	6M
	b)	Discuss about special software techniques that are needed for embedded systems?	6M
7.	a)	With suitable examples explain about the testing in embedded software	6M
	b)	Discuss about functional tests?	6M
8	a)	Provide details of Emulation and Debugging techniques.	6M
	b)	How many kinds of buffers are there and discuss every of them.	6M

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M.Tech. II Semester Regular Examinations, July/August 2014

Hardware Description Languages

(Embedded Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Describe the various operators that are used in verilog	6M
	b)	If A and B are two unsigned variables with A=1100 and B=1001 find the value of following expressions (i) A and B (ii) A^B (iii) |(B) (iv)A SRA 1 (v) A && B	6M
2.	a)	Explain gate delays in gate level modeling	6M
	b)	Draw the logic diagram for priority encoder and write a UDP description for the same	6M
3.	a)	Describe a procedural continuous assignment statements assign, deasign,force and release	6M
	b)	Give a memory of size 64 words, with 8-bits per word; write a verilog code to swap the contents of memory in reverse order. That is transfer of 0 to word 63 word 1 to word 62 and so on.	6M
4.	a)	What are the differences between Melay and Moore machine	6M
	b)	Write a verilog code for a sequence detector using Moore machine which detect the sequence 1011.	6M
5.	a)	Write CaseX and CaseZ in verilog , write verilog code for 4:1 Multiplexer using case statement	6M
	b)	Explain with the help of example, difference between 'fork- join' and 'begin-end' blocks	6M
6.	a)	Explain CMOS switch and write code for it	6M
	b)	Draw Switch Level logic diagram for X-NOR gate with Minimum number of Transistors and write Switch Level Description for the same	6M
7.	a)	Explain the following terms relevant to VHDL. (i) Design Entry (ii) Simulation (iii) Synthesis (iv) Optimization.	6M
	b)	Write about Top-down and Bottom-up design methodologies in IC design	6M
8.	a)	Explain generate and generic statement in VHDL	6M
	b)	What is the importance of wait statement in VHDL explain with example	6M

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M.Tech. II Semester Regular Examinations, July/August 2014

HARDWARE SOFTWARE CO –DESIGN

(Common to VLSISD & Embedded Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Discuss in detail generic co-design methodology?	8M
	b)	Explain the co-design models?	4M
2.	a)	Explain about distributed system co-synthesis?	6M
	b)	Write a short note on Hardware software partitioning?	6M
3.		Explain about prototyping and emulation techniques?	12M
4.	a)	Discuss the architecture for control dominated systems?	6M
	b)	Write short note on system communication infrastructure?	6M
5.		Explain about the compilation technologies?	12M
6.	a)	What is meant by verification? Describe about interface verification?	6M
	b)	Write short notes on verification tools?	6M
7.		Describe various system level specification languages?	12M
8.		Explain about cosyma and lycos system?	12M

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M.Tech. II Semester Regular Examinations, July/August 2014

RADIO FREQUENCY IDENTIFICATION

(Embedded Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Compare and contrast between different Identification Systems	6M
	b)	With a neat diagram briefly explain about different components of an RFID system	6M
2.	a)	Explain in detail about Glass Housing Transponder Construction formats	6M
	b)	Explain in detail about the Differentiation procedures of RFID systems	6M
3.	a)	With neat diagram explain in detail about Electromagnetic Backscatter Coupling	6M
	b)	Explain in detail about Active and Passive Modes of Near Field Communication (NFC)	6M
4.	a)	Explain the Sensor Effect in Surface Wave Transponder	6M
	b)	Explain in detail about the Measurements using Microwave Transponders	6M
5.	a)	Explain the magnetic field operation of the Transponder	6M
	b)	Explain different frequency ranges in RFID systems and their applications	6M
6.	a)	With neat diagram explain Coherent and Non Coherent FSK Receiver	6M
	b)	Briefly explain the modulation procedures with sub carriers	6M
7.	a)	With an example explain the CRC error detection procedure	6M
	b)	Briefly explain the attacks on RFID Systems	6M
8.	a)	Explain briefly about Exxon Mobil Speed Pass RFID System	6M
	b)	Explain about Visa Contactless RFID System	6M

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M.Tech. II Semester Regular Examinations, July/August 2014

TESTING AND TESTABILITY

(Common to Embedded Systems & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Define static and dynamic hazards.	4M
	b)	Explain main flow of event driven simulation.	8M
2.	a)	Define fault equivalence.	4M
	b)	Explain different fault simulation techniques.	8M
3.		Discuss fault models for different functions in detail.	12M
4.	a)	Define the term testability.	4M
	b)	Explain full serial integrated scan architecture in detail.	8M
5.	a)	Explain storage cells for scan design in detail.	6M
	b)	Discuss in detail about the importance of compression techniques.	6M
6.	a)	What is exhaustive testing?	4M
	b)	Explain CSBL architecture.	8M
7.		Explain embedded memory testing model in detail.	12M
8.		Explain in circuit testing.	12M

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