R-11

Code : *1PC421*

**ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET**
**(AUTONOMOUS)**
**M.Tech II Semester Regular December, 2013**

***Scripting Languages for VLSI Design Automation***
**( *VLSI Sys D* )**

**Max. Marks: 60** **Time: 03 Hours**

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**Answer *any five* questions**
**All Questions carry equal marks (12 Marks each)**

1. a. In what way the Scripting languages are useful in VLSI Design Automation? Explain. 6 M

   b. Explain the terms with examples 2x3=6M

   (i) Hashes (ii) Complexities and (iii) Verbs

2. a. Why flashes are called as Associative Arrays? Explain. 6 M

   b. What are the different types of operators? Giving examples, explain about each of them. 6 M

3. What are the Statements and declarations in PERL? Explain in detail. 12 M

4. a. What is the use of file handles? How inter-process communication is made easier with file handlers? Explain 6 M

   b. Discuss various code generators in PERL? 6 M

5. a. Give the Life cycle of a PERL program and explain the same. 6 M

   b. Explain about PERL's object system. 6 M

6. a. Give the PERL Debugger commands and explain about them. 6 M

   b. Explain about scalar-typing methods in PERL. 6 M

7. Explain about PERL Functions with examples. 12 M

8. Write short notes (any two) 6x2=12 M

   i ). Data structures in PERL

   ii).Regular expressions

   iii). CGI

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Code : 1PC321

R-11

**ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET**
**(AUTONOMOUS)**

***M.Tech. II Semester Regular Examinations, December 2013***

***Testing and Testability***

**( *Common ES & VLSI Sys D* )**

**Max. Marks: 60** **Time: 03 Hours**

**Answer *any five* questions**

**All Questions carry equal marks (12 Marks each)**

| | | | |
|---|---|---|---|
| 1. | a. | With examples discuss about gate level event driven simulation. | 06M |
| | b. | Discuss about delay models with examples. | 06M |
| 2. | a. | Construct a circuit that has two independent faults. | 04M |
| | b. | List out the limitations of parallel fault simulation. | 04M |
| | c. | Distinguish between single stuck and multiple stuck at faults. | 04M |
| 3. | a. | Explain about automated test pattern generation for detecting SSF's in combinational circuits. | 06M |
| | b. | Discuss about ATPG vectors, formats, compaction and compression. | 06M |
| 4. | a. | Discuss about Boundary Scan Standards and Compression Techniques. | 06M |
| | b. | Explain about generic boundary scan and full serial integrated scan. | 06M |
| 5. | a. | Give a detail view on syndrome test with examples. | 06M |
| | b. | With neat diagrams discuss about Controllability and Observability. | 06M |
| 6. | a. | Discuss briefly about the following BIST Architectures.<br>(i) STUMPS (ii) CBIST (iii) CEBS (iv) RTD | 08M |
| | b. | Discuss about the need for Test Pattern Generation with examples. | 04M |
| 7. | a. | Discuss about Memory Test Architectures and Techniques. | 06M |
| | b. | Discuss about Types of Memories and Integration. | 06M |
| 8. | | Discuss in detail about JTAG Testing Features. | 12M |

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R-11

**ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET**
**(AUTONOMOUS)**
*M.Tech. II Semester Regular Examinations, December 2013*
***Algorithms for VLSI Design Automation***
*( VLSI Sys D )*

**Max. Marks: 60** **Time: 03 Hours**

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**Answer *any five* questions**
**All Questions carry equal marks (12 Marks each)**

| | | | |
|---|---|---|---|
| 1. | | Explain briefly about VLSI Design Automation Tools? | 12M |
| 2. | | Explain briefly the general purpose methods for combinatorial optimization? | 12M |
| 3. | | Explain the following Algorithms for Constraint-graph Compaction<br>i) The Longest Path in Graphs with Cycles<br>ii) The Bellman-Ford Algorithm | 6x2=12M |
| 4. | a. | What are the general remarks on VLSI Simulation? | 6M |
| | b. | Explain about Switch-level Modeling and Simulation? | 6M |
| 5. | a. | Explain about Binary-decision Diagrams? | 6M |
| | b. | Explain Two-level Logic Synthesis? | 6M |
| 6. | | Explain about Allocation, Assignment and Scheduling of Algorithms in high-level synthesis? | 12M |
| 7. | | Give the Classification of MCM Routing Algorithms? Explain. | 12M |
| 8. | | Write short notes, answer any two<br>i) Dijkstra's Shortest-path Algorithm<br>ii) Physical Design Cycle for FPGAs<br>iii) Channel and global Routing<br>iv) Chip Array and Full Custom approaches | 4x3=12M |

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Code : 1PB323

R-11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech II Semester Regular December, 2013

*DSP Processors and Architectures*
*( Common to DECS, ES & VLSI Sys D )*

**Max. Marks: 60** **Time: 03 Hours**

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**Answer *any five* questions**
**All Questions carry equal marks (12 Marks each)**

1. a. What are the various types of elementary sequences in digital signal processing for analysis purpose? Give their definition and MATLAB representations? 6M
   b. Explain the digital fitters with neat sketches. 6M
2. a. Explain briefly DSP computational errors. 6M
   b. Explain with suitable example the analysis of D/A conversion errors using MATLAB. 6M
3. Explain briefly the DSP computational building blocks with suitable architecture. 12M
4. Explain the following terms: 12M
   i) Pipeline depth
   ii) Branching effect.
   iii) Interrupt effects.
   iv) Stacks
5. a. Explain the memory organization in TMS 320C54XX DSP . 6M
   b. Explain the operation of parallel instruction of TMS 320C54XX. 6M
6. a. Write an algorithm to implement the FIR filter. 6M
   b. Explain how an adaptive filter can be implemented using LMS algorithms. 6M
7. a. Write an algorithm to implement an 8 point (DIT-FFT) on TMS 320C54XX. 6M
   b. Explain the computation of the signal spectrum and how it can be implemented on DSP. 6M
8. a. Explain how DMA is interfaced to a DSP. 6M
   b. Draw the CODEC interface circuit and explain. 6M

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Code : *1PB322*

**R-11**

**ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET**
**(AUTONOMOUS)**
**M.Tech II Semester Regular December, 2013**
***Hardware Software Co –Design***
**( *Common ES & VLSI Sys D* )**

**Max. Marks: 60** **Time: 03 Hours**

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**Answer *any five* full questions**
**All Questions carry equal marks (12 Marks each)**

| | | | |
|---|---|---|---|
| 1. | a. | Explain the architectures related to Co-Design issues. | 6 M |
| | b. | State and explain various Co-Design languages. | 6 M |
| 2. | a. | List and explain any two hardware structure synthesis algorithms. | 8 M |
| | b. | Describe the distributed system Co-Synthesis | 4 M |
| 3. | a. | Differentiate Prototyping and Emulation techniques. | 6 M |
| | b. | Discuss about Prototyping and Emulation environments. | 6 M |
| 4. | a. | What is a Mixed System? Enumerate with the help of an example. | 8 M |
| | b. | Explain the architecture for data dominated systems. | 4 M |
| 5. | | With the help of a diagram explain modern Embedded architecture and discuss about their compilation techniques. | 12 M |
| 6. | a. | Write brief notes on Design Verification. | 6 M |
| | b. | Distinguish between design Specification and Verification. | 6 M |
| 7. | | Describe various system level specification languages. | 12 M |
| 8. | a. | Explain What is Heterogeneous Specification? | 6 M |
| | b. | Write about partitioning sessions in Lycos. | 6 M |

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Code : 1PC322

R-11

**ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET**
**(AUTONOMOUS)**
**M.Tech II Semester Regular December, 2013**

***Low Power VLSI Design***
**( *VLSI Sys D* )**

**Max. Marks: 60** **Time: 03 Hours**

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**Answer *any five* questions**
**All Questions carry equal marks (12 Marks each)**

| | | | |
|---|---|---|---|
| 1. | a. | What is the necessity of low-power VLSI design? | 3M |
| | b. | Explain the relationship between gate delay versus supply voltage. | 3M |
| | c. | With respect to design considerations how low power VLSI design is different from basic VLSI design | 6M |
| 2. | a. | Draw and explain about optimized Twin well BiCMOS fabrication | 6M |
| | b. | Explain about the importance and processes of double poly silicon processes. | 6M |
| 3. | a. | What are the features of SOI technology | 4M |
| | b. | Draw and explain the process sequence of SOI lateral BJT | 8M |
| 4. | a. | Describe the sub threshold current model of MOSFET. | 8M |
| | b. | What are the limitations of MOS device characteristics? | 4M |
| 5. | a. | Draw the circuit for conventional BiCMOS two-input NAND gate. | 6M |
| | b. | What are the basic driver configurations & explain one in detail. | 6M |
| 6. | a. | With the help of circuit diagram explain the working of ESD free BiCMOS Digital circuits | 8M |
| | b. | Write the advantages of ESD Free BiCMOS | 4M |
| 7. | a. | Realize double edge triggered flip flop and explain the operation. | 5M |
| | b. | What are the various quality measures for latches and Flip-Flops and explain one in detail | 7M |
| 8. | a. | What are the consequences of CMOS Floating node? How it can be avoided? | 6M |
| | b. | Draw and explain the operation of SRAM cell | 6M |

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