Code : *1PC323*

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. II-Semester *Regular Examinations, November 2012*
Algorithms for VLSI Design Automation
(*VLSI Sys D*)

Max. Marks: 60   Time: 03 Hours
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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. Explain briefly about VLSI Design Methodologies?   12M

2. Explain briefly the general purpose methods for combinatorial optimization?   12M

3. Explain the following algorithms for Constraint-graph Compaction   6x2=12M
   i)   A Longest-path Algorithm for DAGs
   ii) The Liao- Wong Algorithm

4. a. What are the general remarks on VLSI Simulation?   6M

   Explain Gate-level Modeling and Simulation?   6M

5. a. Explain about Binary-decision diagrams?   6M

   b. Explain Two-level Logic Synthesis?   6M

6. Explain about Allocation, Assignment and Scheduling of Algorithms in high-level synthesis   12M
   Algorithms?

7. Explain the routing algorithm for the Non-Segmented Model, Segmented Model   12M
   and Staggered Model?

8. Write short notes, answer any three   4x3=12M
    i) Computational Complexity
    ii) Kernighan-Lin Partitioning Algorithm
    iii) Graph Algorithms
    iv) Classification of MCM Routing Algorithms
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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. II-Semester *Regular Examinations, November 2012*
DSP Processors and Architectures
(*Common to DECS, ES & VLSI Sys D*)

Max. Marks: 60

Time: 03 Hours

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a. Explain with a block diagram a basic DSP system. What are the advantages and disadvantages of programmable DSP processor? — 6M

   b. For the FIR Filter — 6M

   $$Y(n) = ((x(n) + x(n-1) + x(x-2))/3$$

   Determine the system function, magnitude response function and phase response function.

2. a. Explain A/D Conversion errors in DSP systems. — 6M

   b. Calculate the dynamic range and precision of each of the following number representation formats. — 6M

   i) 24-bit, single-precision, fixed-point format

   ii) 48-bit, double precision, fixed-point format

   iii) a floating point format with a 16-bit mantissa and an 8-bit exponent.

3. a. Design an address generation unit for programmable DSP architecture. — 6M

   b. Explain the implementation of system level parallelism and pipelining using two MAC units. — 6M

4. a. Briefly explain the pipeline programming models in a DSP. — 6M

   b. What is an interrupt? Explain the various interrupts in a DSP. — 6M

5. a. Explain Data addressing modes of TMS 320C54XX processor. — 6M

   b. Explain Interrupts TMS 320C54XX processors. — 6M

6. a. Implement the necessary Algorithm for PID controller using DSP processor. — 6M

   b. Explain the implementation of interpolation filter on a DSP. — 6M

7. a. Implement an FFT algorithm for a bit Reversal Index algorithm. — 6M

   b. Explain about overflow and scaling. — 6M

8. a. Explain the interfacing of memory to a DSP. — 6M

   b. Explain the following I/O peripherals with reference to interfacing — 6M

   (i) interrupts & I/O   (ii) McBSP

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Code : *1PB322*

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. II-Semester *Regular Examinations, November 2012*
Hardware Software Co –Design
(*Common ES & VLSI Sys D*)

Max. Marks: 60   **Time: 03 Hours**

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Answer *any five* full questions
All Questions carry equal marks (12 Marks each)

1.	a.	Discuss a Generic Co-Design methodology.	8 M
	b.	Explain FSMD Model.	4 M
2.		Explain various methodologies involved in Hardware- Software Partitioning.	12 M
3.		What are the various prototyping and emulation techniques? Discuss them briefly.	12 M
4.	a.	With a neat block diagram explain the system communication infrastructure.	7 M
	b.	Explain the architecture for control dominated systems.	5 M
5.		What is meant by compilation? Discuss about practical considerations in a compiler development environment.	12 M
6.	a.	With a suitable example explain the methodology involved in the Co-design Computational model.	8 M
	b.	Write short notes on Interfacing Components.	4 M
7.	a.	Explain design representation for system level synthesis.	6 M
	b.	List and explain system-level specification.	6 M
8.		With a real world example explain about Cosyma system optimization.	12 M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. II-Semester *Regular Examinations, November 2012*
Low Power VLSI Design
(*VLSI Sys D*)

Max. Marks: 60   Time: 03 Hours

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1.	a.	What are the various design limitations on low power ,low voltage circuits	2M
	b.	What is the need of Isolation in BiCMOS devices	3M
	c.	What are the design considerations of bipolar devices in BiCMOS circuits. And explain any one in detail	7M
2.	a.	What are the types of BiCMOS processes	3M
	b.	Define LOCOS & explain with neat diagram.	5M
	c.	Differentiate shallow trench and deep trench isolation techniques	4M
3.	a.	Define about deep submicron technology.	4M
	b.	Draw and explain about SOI CMOS/BiCMOS VLSI	8M
4.	a.	What are the experimental characteristics of sub-half micron MOS devices? Explain how to extract them.	6M
	b.	Explain the concept of MOSFET in a Hybrid-mode environment	6M
5.	a.	What are the various power dissipation mechanisms in CMOS? & explain in detail	4M
	b.	Draw the circuit by conventional BiCMOS for the function $f = (AB+C)'$ and explain the working of the circuit	8M
6.	a.	Write the advantages of Emitter follower driver configuration of BiCMOS circuit.	3M
	b.	What is Latch up?	3M
	c.	How latch up can be avoided in Merged BiCMOS and explain with neat diagram	6M
7.	a.	What are the various themes to evaluate the Latches and Flip flops?	4M
	b.	Draw a transmission-gate based dynamic Filp-flop and explain its operation	8M
8.	a.	Write the advantages of low swing Bus	4M
	b.	Explain how power can be reduced in clock networks and explain in detail	8M

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)
M.Tech. II-Semester *Regular Examinations, November 2012*
Scripting Languages for VLSI Design Automation
(*VLSI Sys D*)

Max. Marks: 60   Time: 03 Hours
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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. A, Define CGI. Briefly discuss strengths and weaknesses of CGI.   4M

   b. With example, explain different types of Java Script operators.   8M

2. a. Explain range operator and relational operators in Perl with an example.   6M

   b. Briefly discuss various compound statements in Perl with an example.   6M

3. a. Explain Arrays of Arrays data structures in Perl with suitable example.   4M

   b. Write short notes on Tied variables in Perl.   8M

4. a. Explain in detail about Named pipes. List its advantages over pipes.   6M

   b. With example, Briefly discuss the creation and destruction of threads   6M

5. a. Explain various phases of Perl program in its life cycle.   6M

   b. Write short notes on Perl environment variables.   6M

6. a. What is Perl Debugger? Why to use Perl Debugger?   6M

   b. Discuss about Debugger Commands in Perl.   6M

7. Write short notes on the following:

   i) Internal Data Types.   6M

   ii) Perl profiler.   6M

8. Write a VB Script that will retrieve principle amount, interest rate, duration of loan   12M
   from a web page. When "Calculate" button is pressed, it should calculate & display
   the simple interest.

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ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

Testing and Testability
(*Common ES & VLSI Sys D*)

Max. Marks: 60   **Time: 03 Hours**

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Answer *any five* questions
All Questions carry equal marks (12 Marks each)

1. a. Bring out the differences in modeling digital circuits at logic level and register level. 06M

   b. Discuss about types of simulation with necessary examples. 06M

2. a. Show that a single output combinational circuit has no independent faults. 04M

   b. Discuss in detail about fault models and fault simulation applications. 04M

   c. Discuss about fault equivalence and fault location. 04M

3. a. With examples discuss about functional testing with specific fault models. 06M

   b. Explain about automated test pattern generation for detecting SSF's in combinational circuits. 06M

4. a. Discuss about the design of Board Level and System Level DFT Approaches. 06M

   b. Discuss about Testability Trade-Offs and Techniques. 06M

5. a. With a neat diagram explain about a 4-bit Signature Analyzer. 06M

   b. Discuss about Scan Architectures and Testing. 06M

6. a. Discuss briefly about the following BIST Architectures. 08M
      (i) CSBL (ii) BEST (iii) RTS (iv) LOCST

   b. Discuss about design for Self-Test at Board Level. 04M

7. a. Discuss about Memory Test Requirements for MBIST. 06M

   b. Discuss about Embedded Memory Testing Model. 06M

8. Discuss in detail about Automatic in Circuit Testing (ICT) 12M

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