R11

Code : 1PC323

M.Tech. II Semester Regular Examinations, July/August 2014

ALGORITHMS FOR VLSI DESIGN AUTOMATION

(VLSI Systems Design)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1. a) Explain in detail, how the structural and logic design are correlated in VLSI design?
   b) Explain the process of generic IC design methodology?
2. a) Distinguish between Depth First search and Breadth first search methods?
   b) Explain briefly the general purpose methods for combinational optimization?
3. a) Explain the simulated annealing using Pseudo code?
   b) Explain the NP completeness and NP hardness?
4. a) What is meant by modeling and simulation?
   b) Explain routing problem's in floor planning methods of VLSI design?
5. a) Explain the assignment and scheduling with example?
   b) Explain the High Level transformations can be carried out on Data Flow Graphs?
6. a) Discuss the basic issue and terminology employed in logic synthesis in VLSI design?
   b) Explain symbolic minimization and encoding problems in logic level synthesis and optimization?
7. a) Explain routing algorithm for the non-segmented model?
   b) Explain MCM physical design?
8. a) Explain the Partitioning and placement in the MCM'S?
   b) Explain the Distribution and routing?

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M.Tech. II Semester Regular Examinations, July/August 2014

DSP PROCESSORS AND ARCHITECTURES

(Common to Embedded Systems & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following

All questions carry equal marks (12 Marks each)

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1. a) Draw the block diagram of DSP systems and write advantages & disadvantages? 6M
   b) Find the convolution of given sequences:
   $x_1(n) = \{3, 4.2, 11, 0, 7, -1, 0, 2\}$, n=0.....7
   $x_2(n) = \{1.2, 3, 0, -0.5.2\}$, n=0.....4 6M
2. a) Explain about fixed point and floating point format representations with an example. 6M
   b) Compare the dynamic range and percentage resolution of a signal that uses:
      i. 16-point fixed point format.
      ii. 32-point floating point format with 14 bit for the mantissa and 8- bit for the exponent. 6M
3. a) Explain the structure of 4 × 4 Broun multiplier. 6M
   b) Write about Data addressing capabilities and explain special addressing modes. 6M
4. a) Explain the following terms in Pipelining:
      i. Interlocking.
      ii. Branching effect. 6M
   b) Distinguish between maskable and non maskable, software and hardware interrupts. 6M
5. a) What are the architectural features of 54XX processor? Explain with a block diagram. 6M
   b) What are various interrupts of 54XX DSP Processors? 6M
6. a) Represent each of the following as 16-bit numbers in the desired Q-notation:
      i) 0.3125 as Q15 number.
      ii) -0.3125 as Q15 number.
      iii) 3.125 as a Q7 number.
      iv) -352 as Q0 number. 6M
   b) Write a program to multiply a Q15 number with a Q15 number to obtain the result in Q15 notation. 6M
7. a) Explain how overflow conditions be avoided by scaling the numbers in FFT computation. 6M
   b) Explain the procedure to generate bit-reversed index for 4-bit and show the result for all possible combinations. 6M
8. a) Draw the memory map representation of TMS 5416 DSP and explain clearly. 6M
   b) Write notes on MCBSPS. 6M

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HARDWARE SOFTWARE CO –DESIGN

(Common to VLSISD & Embedded Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Discuss in detail generic co-design methodology?	8M
	b)	Explain the co-design models?	4M
2.	a)	Explain about distributed system co-synthesis?	6M
	b)	Write a short note on Hardware software partitioning?	6M
3.		Explain about prototyping and emulation techniques?	12M
4.	a)	Discuss the architecture for control dominated systems?	6M
	b)	Write short note on system communication infrastructure?	6M
5.		Explain about the compilation technologies?	12M
6.	a)	What is meant by verification? Describe about interface verification?	6M
	b)	Write short notes on verification tools?	6M
7.		Describe various system level specification languages?	12M
8.		Explain about cosyma and lycos system?	12M

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LOW POWER VLSI DESIGN

(VLSI System Design)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1. a) Explain about the design limitations imposed on low-power, low-voltage circuits pertaining to the following parameters:
   Power supply voltage
   Threshold voltage
   Scaling
   Interconnect wires. 7M
   b) What are the advantages and limitations of Silicon-On-Insulator technology 5M
2. a) Draw the cross sectional diagram of n-well CMOS process and explain the same. Compare this with standard buried collector BiCMOS structure. 6M
   b) How the threshold voltage is adjusted for CMOS structures in BiCMOS devices. 6M
3. a) With schematic diagrams explain about deep submicron process. 6M
   b) Explain how the performance of high speed bipolar transistors is improved in future. 6M
4. a) Explain about Gummel - Poon model of BJT. 6M
   b) Compare VBIC, HICUM and MEXTRAM models of BJT in all respects. 6M
5. Draw the circuit for common emitter BiCMOS driver configuration and discuss its characteristics. 12M
6 a) With suitable circuit explain basic concept and operation of Quasi-Complementary BiCMOS digital circuits. 6M
   b) Write about ESD –free BiCMOS. 6M
7. a) Discuss about the functionality theme and synchronous themes of latches and flip-flops. 6M
   b) Explain the following quality measures for latches and flip-flops.
   Performance measures
   Power dissipation measures. 6M
8. a) Explain in detail how power can reduced in clock-networks? 6M
   b) Discuss about low power techniques for SRAM. 6M

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M.Tech.. II Semester Regular Examinations, July/August 2014

Scripting Languages for VLSI Design Automation

(VLSI Sys D)

Max. Marks: 60 **Time: 03 Hours**

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Answer *any five* questions

All Questions carry equal marks (12 Marks each)

1. a. Scripting languages such as Perl, VB Script and Java Script represent a very different style of programming than system programming languages such as C, C++ and Java. Justify your answer. 6M

   b. Discuss various looping statements in VB Script with suitable examples. 6M

2. Write short notes on following: 12M

   i) Substitution operator.

   ii) Matching operator.

   iii) Bare Blocks.

3. a. Briefly discuss about Hashes of Arrays data structures in Perl. 6M

   b. What are modules in Perl? Explain about creating the modules. 6M

4. a. Explain sockets form of IPC in detail? List its advantages over other form of IPC mechanisms. 8M

   b. With suitable example, Explain Creation and destruction of Threads. 4M

5. a. With neat diagram, Explain the Life Cycle of Perl Program. 6M

   b. Write short notes on command processing in Perl. 6M

6. a. What do you mean by Breakpoints in Perl Debugger? Briefly explain. 6M

   b. Briefly explain about Debugger support. 6M

7. Discuss the following with an example: 12M

   i) Extending Perl (Using C from Perl).

   ii) Embedding Perl (Using Perl from C).

8. Write a Java Script for the following and briefly explain. 12M

   i) Embedding the Java Script in the HTML file.

   ii) Java Script in a separate file and include in the HTML file.

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TESTING AND TESTABILITY

(Common to Embedded Systems & VLSISD)

Time: 3 hours **Max Marks: 60**

Answer any FIVE of the following
All questions carry equal marks (12 Marks each)

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1.	a)	Define static and dynamic hazards.	4M
	b)	Explain main flow of event driven simulation.	8M
2.	a)	Define fault equivalence.	4M
	b)	Explain different fault simulation techniques.	8M
3.		Discuss fault models for different functions in detail.	12M
4.	a)	Define the term testability.	4M
	b)	Explain full serial integrated scan architecture in detail.	8M
5.	a)	Explain storage cells for scan design in detail.	6M
	b)	Discuss in detail about the importance of compression techniques.	6M
6.	a)	What is exhaustive testing?	4M
	b)	Explain CSBL architecture.	8M
7.		Explain embedded memory testing model in detail.	12M
8.		Explain in circuit testing.	12M

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