

Hall Ticket Number :									
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<b>R-20</b>
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**Code: 20AE5AT**

III B.Tech. I Semester Regular Examinations Dec 2022/Jan 2023

**Human Resource Management**

( Common to CE, EEE & ECE )

Max. Marks: 70

Time: 3 Hours

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- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)  
2. In Part-A, each question carries **Two mark**.  
3. Answer **ALL** the questions in **Part-A** and **Part-B**

**PART-A**

**(Compulsory question)**

- |  | CO | BL |
|--|----|----|
| 1. Answer all the following short answer questions ( 5 X 2 = 10M ) |    |    |
| a) List the functions of HRM.                                      | 1  | 1  |
| b) Define Human Resources Information Systems.                     | 1  | 1  |
| c) Define Selection.   | 1  | 1  |
| d) Define Career Development.                                      | 1  | 1  |
| e) Define Performance Appraisal.                                   | 1  | 1  |

**PART-B**

**Answer five questions by choosing one question from each unit ( 5 x 12 = 60 Marks )**

- |  | Marks | CO | BL |
|--|-------|----|----|
| <b>UNIT-I</b>  |       |    |    |
| 2. Discuss in detail the competitive challenges influencing HRM.   | 12M   | 1  | 2  |
| <b>OR</b>  |       |    |    |
| 3. Describe in detail, the ethical aspects of HRM.   | 12M   | 1  | 2  |
| <b>UNIT-II</b>   |       |    |    |
| 4. Discuss in detail, the significance of Human Resources Planning with specific reference to the IT Industry. | 12M   | 2  | 2  |
| <b>OR</b>  |       |    |    |
| 5. Discuss in detail, the various Factors affecting Job Design and the approaches to Job design.               | 12M   | 2  | 2  |
| <b>UNIT-III</b>  |       |    |    |
| 6. Discuss in detail, the process and sources of recruitment.  | 12M   | 3  | 2  |
| <b>OR</b>  |       |    |    |
| 7. Discuss in detail, the various barriers to effective selection.   | 12M   | 3  | 2  |
| <b>UNIT-IV</b>   |       |    |    |
| 8. Discuss in detail the various methods of training.  | 12M   | 4  | 2  |
| <b>OR</b>  |       |    |    |
| 9. Describe the various impediments that can be a barrier for effective training.                              | 12M   | 4  | 2  |
| <b>UNIT-V</b>  |       |    |    |
| 10. Describe in detail, the concept of wage policy in the Indian Context.                                      | 12M   | 5  | 2  |
| <b>OR</b>  |       |    |    |
| 11. Discuss in detail, the importance and approaches to effective Industrial Relations.                        | 12M   | 5  | 2  |

\*\*\* End \*\*\*

Hall Ticket Number :

**R-20**

**Code: 20A453T**

III B.Tech. I Semester Regular Examinations Dec 2022/Jan 2023

**Microprocessors and Interfacing**

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

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- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)  
2. In Part-A, each question carries **Two mark**.  
3. Answer **ALL** the questions in **Part-A** and **Part-B**

**PART-A**

(Compulsory question)

- |  | CO | BL |
|--|----|----|
| 1. Answer all the following short answer questions ( 5 X 2 = 10M )                   |    |    |
| a) Compare 8085 with 8086 in terms of instruction set?                               | 1  | 2  |
| b) Differentiate near jump and far jump in 8086?                                     | 2  | 4  |
| c) List the any two differences between RAM and ROM?                                 | 3  | 1  |
| d) What is fully nested priority mode in 8259A?                                      | 4  | 1  |
| e) Write any two differences between synchronous and asynchronous data transmission? | 5  | 4  |

**PART-B**

Answer *five* questions by choosing one question from each unit (5 x 12 = 60 Marks)

- |   | Marks | CO | BL |
|---|-------|----|----|
| <b>UNIT-I</b>   |       |    |    |
| 2. a) Describe the architecture of 8085 with neat diagram                                     | 6M    | 1  | 1  |
| b) Describe the addressing modes of 8086 with examples  | 6M    | 1  | 1  |
| <b>OR</b>   |       |    |    |
| 3. a) Describe the architecture of 8086 with neat block diagram                               | 6M    | 1  | 1  |
| b) Illustrate the interrupt and interrupt process in 8086 family processors?                  | 6M    | 1  | 2  |
| <b>UNIT-II</b>  |       |    |    |
| 4. a) Draw internal architecture of 8257 DMA controller and explain its programming features. | 6M    | 2  | 2  |
| b) Distinguish SRAM and DRAM Memory Cells.  | 6M    | 2  | 4  |
| <b>OR</b>   |       |    |    |
| 5. a) Explain with neat diagram to interface 8257 with 8086 processor?                        | 6M    | 2  | 6  |
| b) Interface 16KX8 RAM and 16KX8 ROM to 8086. Give suitable scheme for address mapping.       | 6M    | 2  | 6  |

<b>UNIT-III</b>
-----------------

- |  |    |   |   |
|--|----|---|---|
| 6. a) Explain the different operational modes of 8255.                   | 6M | 3 | 2 |
| b) Describe with neat diagram how DAC is interfaced with 8086 processor? | 6M | 3 | 6 |

**OR**

- |  |    |   |   |
|--|----|---|---|
| 7. a) Write a program to interface stepper motor to 8086 microprocessor. | 6M | 3 | 4 |
| b) Discuss about the control word for 8255                               | 6M | 3 | 2 |

<b>UNIT-IV</b>
----------------

- |   |    |   |   |
|---|----|---|---|
| 8. a) Explain the architecture of 8259 with neat diagram              | 6M | 4 | 2 |
| b) Explain with neat diagrams the various modes of operation of 8253? | 6M | 4 | 2 |

**OR**

- |  |    |   |   |
|--|----|---|---|
| 9. a) Draw the control word format of 8259 and explain?        | 6M | 4 | 2 |
| b) Draw the functional diagram of 8254 and explain each block? | 6M | 4 | 2 |

<b>UNIT-V</b>
---------------

- |  |    |   |   |
|--|----|---|---|
| 10. a) Draw the control word format of 8251?                           | 6M | 5 | 2 |
| b) With the help of neat diagram explain the bus structure of IEEE 488 | 6M | 5 | 2 |

**OR**

- |   |    |   |   |
|---|----|---|---|
| 11. a) Draw and explain various DTE and DCE connection using RS232C?      | 6M | 5 | 2 |
| b) With the help of neat diagram explain handshaking signals of IEEE 488? | 6M | 5 | 2 |

\*\*\* End \*\*\*

Hall Ticket Number :

R-20

Code: 20A45BT

III B.Tech. I Semester Regular Examinations Dec 2022/Jan 2023

**Nano Electronics**

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

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- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)  
2. In Part-A, each question carries **Two mark**.  
3. Answer **ALL** the questions in **Part-A** and **Part-B**

**PART-A**

(Compulsory question)

- |   |     |    |
|---|-----|----|
| 1. Answer <b>all</b> the following short answer questions ( 5 X 2 = 10M ) | CO  | BL |
| a) What are the likely impacts of nanotechnology?                         | CO1 | L1 |
| b) Define Quantum well.   | CO2 | L2 |
| c) List any two quantum electronic devices.                               | CO3 | L2 |
| d) What is the tunneling element?   | CO4 | L1 |
| e) What is the Debye length?  | CO5 | L2 |

**PART-B**

Answer *five* questions by choosing one question from each unit ( 5 x 12 = 60 Marks )

Marks CO BL

**UNIT-I**

2. Describe the following components of Scanning Electron Microscope
- |               |                      |     |     |   |
|---------------|----------------------|-----|-----|---|
| a) Scan Coils | b) Electron Detector | 12M | CO1 | 2 |
|---------------|----------------------|-----|-----|---|

**OR**

- |  |    |     |   |
|--|----|-----|---|
| 3. a) With schematic, describe atomic force microscopy.      | 6M | CO1 | 2 |
| b) With schematic, describe Secondary Ion Mass Spectrometry. | 6M | CO1 | 2 |

**UNIT-II**

- |  |    |     |     |
|--|----|-----|-----|
| 4. a) With a drawing, describe the principles of nano imprint lithography. | 6M | CO2 | 2,3 |
| b) Illustrate the split-gate technology                                    | 6M | CO2 | 3   |

**OR**

- |  |    |     |     |
|--|----|-----|-----|
| 5. a) Discuss the model of semiconductor hetero structures using a clean sketch. | 6M | CO2 | 1,2 |
| b) Explain the basics of lithography with a drawing.                             | 6M | CO2 | 2   |

<b>UNIT-III</b>
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6. a) Describe in depth the concept of Quantum cellular automata. 6M CO3 2,3  
 b) Describe the quantum dot array in detail. 6M CO3 2,3

**OR**

7. a) Explain the concept and operation of Electron-spin transistor using the appropriate schematics. 6M CO3 1,3  
 b) Shortly describe the short channel MOS transistor. 6M CO3 2,3

<b>UNIT-IV</b>
----------------

8. a) Describe in detail the design of basic Logic gates Inverter and OR gate based on RTDS. 6M CO4 2,3  
 b) Explain the Coulomb Blockade 6M CO4 1,2

**OR**

9. a) Elucidate SET Circuit Design for Memory circuits 6M CO4 3  
 b) Illustrate the Performance of the Single-Electron Transistor. 6M CO4 2,4

<b>UNIT-V</b>
---------------

10. a) Describe how Reliability Acts as limiting factors of integrated circuits. 6M CO5 2  
 b) Explain the hardware requirements of nano systems 6M CO5 3

**OR**

11. a) Elucidate how Nano systems act as information processing machines 6M CO5 4  
 b) Explain two important limitations of Integrated electronics? 6M CO5 2

\*\*\* End \*\*\*

Hall Ticket Number :

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**R-20**

**Code: 20A45DT**

III B.Tech. I Semester Regular Examinations Dec 2022/Jan 2023

**Pulse and Digital Circuits**

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)

2. In Part-A, each question carries **Two mark**.

3. Answer **ALL** the questions in **Part-A** and **Part-B**

**PART-A**

(Compulsory question)

- |  | CO | BL |
|--|----|----|
| 1. Answer all the following short answer questions ( 5 X 2 = 10M )                         |    |    |
| a) Name the signals which are commonly used in pulse circuits and define any five of them. | 1  | 1  |
| b) Distinguish between comparators and clipping circuits?                                  | 2  | 2  |
| c) Briefly discuss about the Commutating Capacitors?                                       | 2  | 1  |
| d) Compare voltage and current time base generators  | 3  | 2  |
| e) Differentiate between logic gates and sampling gates                                    | 3  | 1  |

**PART-B**

Answer *five* questions by choosing one question from each unit ( 5 x 12 = 60 Marks )

Marks CO BL

**UNIT-I**

- |   |    |   |   |
|---|----|---|---|
| 2. a) Derive an expression for output of a RC differentiator circuit when its input is exponential signal. Determine the transmission error | 8M | 1 | 1 |
| b) Derive the gain response of a RC high pass Circuit when sinusoidal signal as input.  | 4M | 1 | 2 |

**OR**

- |  |    |   |   |
|--|----|---|---|
| 3. a) A 10 kHz symmetrical square wave whose peak to peak amplitude is 2V is impressed upon a high pass circuit whose lower 3dB frequency is 5Hz. Calculate and sketch the output waveform in particular what is the peak to peak amplitude. | 5M | 1 | 3 |
| b) Show that how RC low pass circuit acts as an integrator   | 7M | 1 | 1 |

**UNIT-II**

- |   |    |   |   |
|---|----|---|---|
| 4. a) Draw the circuit diagram for positive clamper circuit and explain its principle of operation. | 6M | 2 | 1 |
|---|----|---|---|

- b) Discuss the function of series diode and shunt diode clipping circuits? How can the clipping level shifted to reference voltage? Explain? 6M 2 2

**OR**

5. a) Explain the working of transistor clipper. 5M 2 2
- b) With neat circuit diagram, explain the working of an emitter coupled clipper. 7M 2 1

**UNIT-III**

6. a) Explain the function of Astable multivibrator with waveforms 8M 2 1
- b) Sketch the output waveform of a Schmitt trigger circuit for sine wave input of 12V peak to peak if UTP =5V and LTP= 3V. 4M 2 2

**OR**

7. a) Explain the principle of operation of Bi-stable multivibrators. 8M 2 3
- b) A fixed bias Bi-stable multivibrator circuit uses a DC supply of  $\pm 12$  V,  $R_C=2k$  ,  $R_1=10k$  and  $R_2=47k$  . NPN silicon transistor with  $V_{CE(sat)} = 0.1$  V,  $V_{BE (sat)} = 0.7$  V and  $h_{FE} (min)=30$  are used. 4M 2 2

**UNIT-IV**

8. a) Explain the working of a principle of Bootstrap sweep circuit and derive expression for the slope sweep error. 6M 3 1
- b) Define the three errors that occur in a sweep circuit and obtain an expression for these errors for an exponential sweep circuit. 6M 3 2

**OR**

9. a) Draw and clearly indicate the restoration time and flyback time on the typical waveform of a time base voltage. 4M 3 3
- b) Discuss about the linearly correction through adjusting of driving waveform 8M 3 2

**UNIT-V**

10. a) Design and verify the truth table of two input DTL NAND gate with the circuit diagram 6M 4 6
- b) Compare unidirectional and bidirectional sampling gates 6M 3 2

**OR**

11. a) Compare logic families in detail. 6M 3 3
- b) Explain about four diode sampling gate. 6M 3 2

\*\*\* End \*\*\*

Hall Ticket Number :

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**R-20**

**Code: 20A451T**

III B.Tech. I Semester Regular Examinations Dec 2022/Jan 2023

**VLSI Design**

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

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- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)  
2. In Part-A, each question carries **Two mark**.  
3. Answer **ALL** the questions in **Part-A** and **Part-B**

**PART-A**

(Compulsory question)

1. Answer **all** the following short answer questions ( 5 X 2 = 10M )
- |  | CO  | BL  |
|--|-----|-----|
| a) List the basic process for IC fabrication                   | CO1 | BL4 |
| b) Define Threshold voltage in CMOS?                           | CO2 | BL1 |
| c) Why NMOS technology is preferred more than PMOS technology? | CO3 | BL1 |
| d) What is Stick Diagram?                                      | CO4 | BL1 |
| e) What are the two types of Layout design rules?              | CO5 | BL1 |

**PART-B**

Answer **five** questions by choosing one question from each unit ( 5 x 12 = 60 Marks )

Marks CO BL

**UNIT-I**

2. Explain in detail about the steps involved in CMOS IC fabrication process with essential diagrams. 12M CO1 BI2

**OR**

3. Draw the  $I_{ds}-V_{ds}$  relationship curve and discuss in detail about its role in the MOS design equations 12M CO1 BI6

**UNIT-II**

4. a) Write a short note on "2 $\mu$ m, CMOS design rules". 6M CO2 BI1  
b) Draw the circuit diagrams and the corresponding stick diagrams for nMOS and CMOS inverters 6M CO2 BI1

**OR**

5. a) Explain with diagram CMOS inverter operation. 6M CO2 BI2  
b) What are the limitations of scaling of MOS Circuits 6M CO2 BI1



**UNIT-III**

6. a) Discuss about the inverter delay 4M CO3 BI4  
 b) Derive an expression for sheet resistance ( $R_s$ ) and apply the concept for calculation of sheet resistance for CMOS inverter 8M CO3 BI1

**OR**

7. a) What are the alternate gate circuits are available? Explain briefly with suitable sketch 6M CO3 BI2  
 b) With a detailed step by step procedure design and draw the AND-OR-INVERT form complex in CMOS logic circuit for the output equation  $Y = \overline{A+B+C} + \overline{A+B} + \overline{A+C} + \overline{B+C}$  6M CO3 BI5

**UNIT-IV**

8. a) Describe the nature of a parity generator and explain its structured design approach. 6M CO4 BI2  
 b) Explain in detail about design flow of FPGA. 6M CO4 BI2

**OR**

9. a) Give the subsystem design considerations of a four-bit adder 6M CO4 BI4  
 b) Explain step-by-step subsystem design approach. Consider an example. 6M CO4 BI2

**UNIT-V**

10. a) Explain the concept of design verification and design capture tools used in VHDL synthesis. 9M CO5 BI2  
 b) Write a short note on Built in self-test 3M CO5 BI1

**OR**

11. a) What is the need of testability? Explain design for testability. 6M CO5 BI1  
 b) Describe briefly about chip level test techniques 6M CO5 BI5

\*\*\* End \*\*\*

Hall Ticket Number :

R-20

Code: 20A452T

III B.Tech. I Semester Regular Examinations Dec 2022/Jan 2023

### Control Systems

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)

2. In Part-A, each question carries **Two mark**.

3. Answer **ALL** the questions in **Part-A** and **Part-B**

#### PART-A

(Compulsory question)

1. Answer **all** the following short answer questions ( 5 X 2 = 10M )
- |   |     |    |
|---|-----|----|
|   | CO  | BL |
| a) What are the limitations of transfer function approach?  | CO1 | L3 |
| b) The damping ratio of the system is 0.75 and the natural frequency of oscillation is 12 rad/sec. Determine the overshoot and peak time. | CO2 | L3 |
| c) How closed loop frequency response is determined from open loop frequency response using M and N circles?                              | CO3 | L3 |
| d) What is compensation? What are the different types of compensators?  | CO4 | L3 |
| e) Write the general form the state transition matrix   | CO5 | L1 |

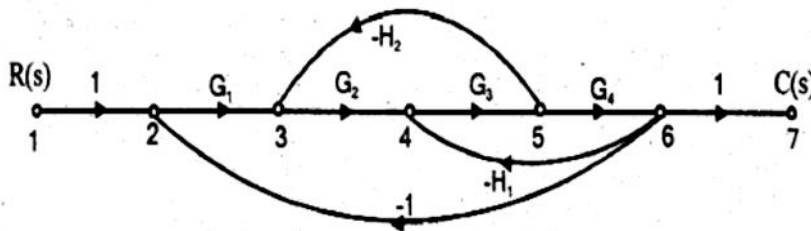
#### PART-B

Answer **five** questions by choosing one question from each unit ( 5 x 12 = 60 Marks )

Marks CO BL

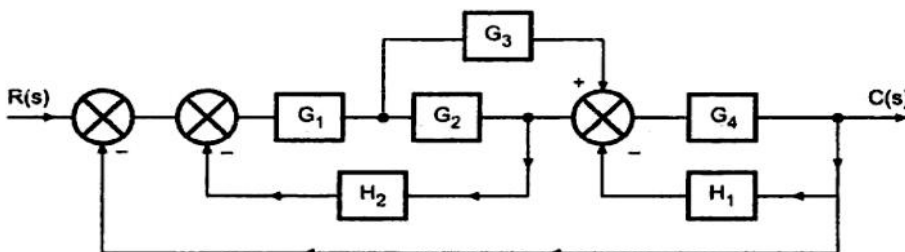
#### UNIT-I

2. a) Find the overall gain  $C(s)/R(s)$  for the signal flow graph shown in fig.



6M CO2 L3

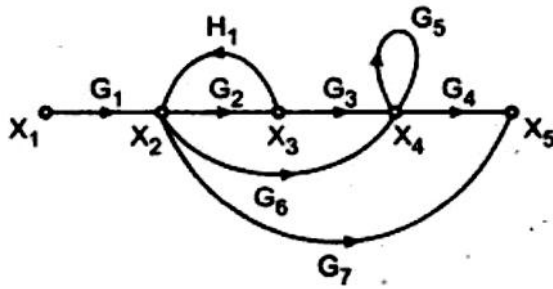
- b) Reduce the block diagram to its canonical (simple) form and hence obtain the equivalent transfer function  $C(s)/R(s)$ .



6M CO3 L3

OR

3. a) For the signal flow graph shown in following fig. determine  $x_5/x_1$ . Use Mason's gain formula.



8M CO2 L3

- b) Write the block diagram reduction techniques.

4M L1

### UNIT-II

4. A second order system is given by  $\frac{C(s)}{R(s)} = \frac{25}{s^2 + 6s + 25}$ . Find its rise time, peak time, peak overshoot and settling time if subjected to unit step input. Also calculate expression for its output response.

12M CO2 L3

**OR**

5. a) Discuss about steady state error constants.  
 b) Open loop T.F of unity feedback system is  $G(s) = \frac{K}{(1+Ts)s}$  where K and T are constants. Determine factor by which gain "K" should be multiplied so that overshoot of unit step response be reduced from 75% to 25%.

6M CO2 L2

6M CO2 L3

### UNIT-III

6. a) Construct the Routh array and determine the stability of the system represented by the characteristic equation  $s^5 + s^4 + 2s^3 + 2s^2 + 3s + 5 = 0$ . Comment on the location of the roots of characteristic equation.  
 b) By means of RH criterion determine the stability of the system represented by the characteristic equation  $S^4 + 2S^3 + 8S^2 + 4S + 3 = 0$

6M CO3 L3

6M CO3 L3

**OR**

7. Sketch the root locus plot of the system whose open loop transfer function is given by

$$G(s)H(s) = \frac{K}{s(s+4)(s^2+4s+13)}$$

12M CO3 L4

<b>UNIT-IV</b>
----------------

8. a) What are the different types of compensators available?  
Explain briefly.

4M CO4 L3

b) Sketch the Bode plot for the system with the transfer function

$$G(s)H(s) = \frac{10}{s(1+0.5s)(1+0.1s)}$$

8M CO4 L3

**OR**

9. The open-loop transfer function of unity feedback system is given by  $G(s) = \frac{1}{s^2(1+s)(1+2s)}$ . Sketch the polar plot and determine the gain margin and phase margin.

12M CO4 L4

<b>UNIT-V</b>
---------------

10. For the given system  $\dot{X} = Ax + Bu$   
where

$$A = \begin{bmatrix} 1 & 2 & 1 \\ 0 & 1 & 3 \\ 1 & 1 & 1 \end{bmatrix}; \quad B = \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix}$$

Find the characteristic equation of the system and its roots

12M CO2 L3

**OR**

11. Find the controllability and observability for the following system model.

$$\dot{X}(t) = \begin{bmatrix} 0 & 1 \\ -6 & -2 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + u(t) \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

$$Y(t) = \begin{bmatrix} 3 & 0 \end{bmatrix} X(t)$$

12M CO3 L3

\*\*\* End \*\*\*

Hall Ticket Number :

**R-20**

**Code: 19A454T (SS)**

III B.Tech. I Semester Regular Examinations Dec 2022/Jan 2023

**Digital Communications**

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

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- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)  
2. In Part-A, each question carries **Two mark**.  
3. Answer **ALL** the questions in **Part-A** and **Part-B**

**PART-A**

(Compulsory question)

- |   |                 |    |    |
|---|-----------------|----|----|
| 1. Answer <b>all</b> the following short answer questions | ( 5 X 2 = 10M ) | CO | BL |
| a) What is Quantization noise?                            |                 | 1  | L1 |
| b) Define Adaptive dcpm.                                  |                 | 2  | L2 |
| c) Write the equation of Shannon Heartly.                 |                 | 3  | L1 |
| d) Write the properties of cyclic codes                   |                 | 4  | L1 |
| e) Define code rate in convolutional encoder.             |                 | 5  | L1 |

**PART-B**

Answer **five** questions by choosing one question from each unit ( 5 x 12 = 60 Marks )

Marks CO BL

**UNIT-I**

- |   |    |   |    |
|---|----|---|----|
| 1. a) Write in detail about the drawbacks of Delta modulation | 6M | 1 | L2 |
| b) Describe the Bandwidth requirements of PCM                 | 6M | 1 | L2 |

**OR**

- |   |    |   |    |
|---|----|---|----|
| 2 a) Explain the need of Adaptive Delta modulation with neat sketch | 6M | 1 | L3 |
| b) Describe in detail about Differential PCM                        | 6M | 1 | L1 |

**UNIT-II**

- |  |    |   |    |
|--|----|---|----|
| 3. a) Explain in detail about the Non-Coherent detection of FSK          | 6M | 2 | L1 |
| b) Describe about the generation of Phase shift Keying with neat diagram | 6M | 2 | L2 |

**OR**

- |  |    |   |    |
|--|----|---|----|
| 4. a) Explain in detail about M-ary signaling                              | 6M | 2 | L2 |
| b) Describe the BASK modulation technique with the help of a neat diagram. | 6M | 2 | L2 |

**UNIT-III**

- |  |     |   |    |
|--|-----|---|----|
| 5 Define the following i)Information ii) Entropy iii) Rate of Information iv) Channel Capacity | 12M | 3 | L2 |
|--|-----|---|----|

**OR**

6. State and prove the properties of Mutual Information 12M 3 L1

**UNIT-IV**

- 7 a) Describe about matrix description of Linear Block Codes 6M 4 L2  
 b) Describe about Error detection and correction capabilities of Linear block codes 6M 4 L2

**OR**

8. A DMS transmitting five symbols  $X_1$ ,  $X_2$ ,  $X_3$ ,  $X_4$ , and  $X_5$  with Probabilities 0.4, 0.1, 0.2, 0.1, 0.2. Then find efficiency and Variance  
 i) By Placing the Combined symbol as high as possible  
 ii) By Placing the Combined symbol as low as possible 12M 4 L3

**UNIT-V**

- 9 a) Describe the Algebraic Structure of Cyclic codes 6M 5 L1  
 b) Explain the Syndrome circuit for Cyclic codes 6M 5 L1
10. For a (2,1,3) Convolution encoder if  $g_1=[1\ 1\ 0]$   $g_2=[1\ 0\ 1]$  then draw the TREE diagram 12M 5 L2

\*\*\* End \*\*\*