Hall Ticket Number :										

R-11 / R-13

Code: 1G457

III B.Tech. I Semester Supplementary Examinations November 2018

Computer System Architecture

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1.	a)	Draw and explain the block diagram of a computer.	9M
	b)	Convert the $(246)_{10}$ to Binary	5M
2.		What is bus? Draw the figure to show how functional units are interconnected using a bus and explain it	14M
3.	a)	Explain the basic computer instruction formats	7M
	b)	Explain the different types of addressing modes	7M
4.	a)	Explain address sequencing with neat diagram.	8M
	b)	Discuss the design of control unit?	6M
5.		Draw and explain the addition and subtraction of floating point numbers	14M
6.	a)	Explain the block diagram of Associative memory	8M
	b)	Explain about the segmented page mapping	6M
7.	a)	Explain how to access I/O devices in a system	7M
	b)	Discuss about Direct-Memory access	7M
8.	a)	Explain the characteristics of multiprocessors	9M
	b)	What is Cache Coherence?	5M

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Hall Ticket Number :										

R-11 / R-13

Code: 1G353

III B.Tech. I Semester Supplementary Examinations November 2018

Digital IC Applications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks each**)

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1.	a)	Discuss about CMOS dynamic electrical behavior with characteristics	6M
	b)	Define logic levels, noise margins & write the importance of noise margins in different IC logic families.	8M
2.	a)	What is the necessity of separate interfacing circuit to connect CMOS gate to TTL gate? Draw the interface circuit and explain the operation	8M
	b)	Design a transistor circuit of 2 input ECL NOR gate. Explain the operation with the help of function table.	6M
3.	a)	Discuss the steps in VHDL design flow.	7M
	b)	What are different data types available in VHDL? Explain.	7M
4.	a)	Explain the structural design elements of VHDL	7M
	b)	Write a VHDL code for 4 bit binary Ripple Carry Adder in Structural model with neat logic diagram	7M
5.	a)	Design a full adder using two half adders. Write VHDL program for the above Implementation using case statement	7M
	b)	Distinguish Concurrent Vs Sequential signal assignment statement.	7M
6.	a)	Discuss any 3 sequential statements with an example each.	7M
	b)	Explain Inertial delay model and Transport delay model in VHDL.	7M
8.		Define barrel shifter. Write the VHDL program for 16-bit barrel shifters and draw the neat diagram.	14M
10.	a)	Distinguish between static and dynamic RAM	7M
	b)	Describe the read and write operations of dynamic RAM cell.	7M

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Hall Ticket Number :										

R-11 / R-13

Code: 1G352

III B.Tech. I Semester Supplementary Examinations November 2018

Linear IC Applications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) Why the level translator is called as an emitter follower and explain its operation. 7M

   b) Derive an expression for voltage gain & input impedance of any one differential amplifier configuration. 7M

2. a) Explain the block diagram representation of a typical Op-Amp. 5M

   b) Discuss the DC characteristics of an Op-Amp in detail. 9M

3. a) Describe the operation of three Op – Amp instrumentation amplifier and its application. 7M

   b) Design an Adder – Subtractor circuit for the given output $V_o = 2V_1-3V_2+4V_3-5V_4$ 7M

4. a) What is the difference between a normal diode rectifier and a precision rectifier? Explain with neat diagrams. 7M

   b) Design an Op-Amp Monostable multi for an output pulse duration of 1ms. 7M

5. a) How can you differentiate wide band pass filters and narrow band pass filters? Discuss the design of any one of the above filters. 8M

   b) Design a second order low pass filter at a high cutoff frequency of 1KHz. 6M

6. a) Draw and explain the monostable operation of 555 timer. 7M

   b) Draw the block diagram of 565 PLL and explain its principle of operation. 7M

7. a) Explain in detail with a neat circuit diagram, the operation of a Parallel comparator type A/D converter. 7M

   b) Explain any two DAC techniques. 7M

8. a) Explain any two applications of Multipliers. 7M

   b) Explain the operation of Balanced Modulator with neat sketch. 7M

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