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<b>R-13</b>
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**Code: 1G352**

III B.Tech. I Semester Supplementary Examinations February 2021

**Linear IC Applications**

( Electronics and Communication Engineering )

Max. Marks: 70

Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) What is the purpose of Differential amplifier and explain the low frequency small signal analysis of it. 7M  
b) Explain the difference between constant current bias and current mirror. 7M
2. a) Design a summing amplifier to add four DC input voltages. The output of this circuit must be equal to three times the negative sum of the inputs. 7M  
b) Explain the need and operation of lossy integrator. 7M
3. a) Explain the difference between integrator and differentiator and give one application of each. 7M  
b) Draw and explain the operation of a current to voltage converter. If 741C is used, what is the lowest value of current that may be measured? 7M
4. a) What is the difference between a normal diode rectifier and a precision rectifier? Explain with neat diagrams. 7M  
b) Design an Op-Amp Monostable multi for an output pulse duration of 1ms. 7M
5. a) How can you differentiate wide band pass filters and narrow band pass filters? Discuss the design of any one of the above filters. 7M  
b) Design a second order low pass filter at a high cutoff frequency of 1KHz. 7M
6. a) Draw and explain the monostable operation of 555 timer. 7M  
b) Draw the block diagram of 565 PLL and explain its principle of operation. 7M
7. a) Explain the working principle of Inverted R-2R DAC with a neat diagram. 7M  
b) Explain the working principle of parallel comparator type ADC with a neat diagram. 7M
8. a) Draw and explain a sample and hold circuit. 7M  
b) Discuss the applications of analog switches. 7M

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<b>R-13</b>
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**Code: 1G457**

III B.Tech. I Semester Supplementary Examinations February 2021

**Computer System Architecture**

( Electronics and Communication Engineering )

Max. Marks: 70

Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) Describe with neat sketch the functional units of computers.  
b) Explain in brief complements in data representation.
2. a) How information transfer from one register to another register? Explain.  
b) List the basic computer instructions. Sketch the basic computer instructions.
3. List and explain instruction formats in brief.
4. a) Describe the symbolic microinstructions.  
b) What is the need of decoding of microoperations fields? Explain.
5. How addition and subtraction with signed magnitude data perform? Explain with flow chart.
6. a) Describe the memory hierarchy in computer system.  
b) What is meant by memory address map? Explain.
7. a) Discuss about Direct Memory Access.  
b) Draw block diagram of a computer with I/O Processor. Describe.
8. a) Describe delayed load in RISC pipeline.  
b) What is cache coherence? Explain.

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<b>R-13</b>
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**Code: 1G353**

III B.Tech. I Semester Supplementary Examinations February 2021

**Digital IC Applications**

( Electronics and Communication Engineering )

Max. Marks: 70

Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) List different types of CMOS logic families and compare with different parameters. 5M  
b) Explain about CMOS dynamic electrical behavior. 9M
2. a) Explain the transistor switching operation of 2 input LS-TTL NAND with neat circuit diagram and truth tables. 7M  
b) Distinguish between CMOS logic and TTL logic circuits. 7M
3. a) Explain about various Data types used in VHDL. 7M  
b) Describe the design flow diagram of VHDL. 7M
4. a) With an example, mention the structural design elements of VHDL? 7M  
b) Discuss any Three sequential statements with relevant examples. 7M
5. a) Design 4 to 16 decoder using standard ICs. 7M  
b) Write a VHDL program for 4-bit Comparator. 7M
6. a) Write short notes on comparators. 7M  
b) What is the purpose of Wait-statement in VHDL? 7M
7. Draw and explain the logical operation of SR, JK, D, and T Flip-flops. 14M
8. Draw the basic cell structure of Dynamic RAM. What is the necessity of refresh cycle? Explain the timing requirements of refresh operation. 14M

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