Hall Ticket Number :										

R-11 / R-13

Code: 1G457

III B.Tech. I Semester Supplementary Examinations October 2020

Computer System Architecture

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) Name basic operational concepts in computer. Explain in detail
   b) How a number is represented as floating point representation? Illustrate with suitable example.

2. a) What is the need of three state buffers? Explain
   b) Draw and describe flow chart for interrupt cycle.

3. a) Describe the register stack.
   b) How many types of interrupts are used for break the normal execution of a program?

4. a) What is format of microinstruction for the control memory? Explain.
   b) Explain fetch routine in control memory.

5. a) Perform the multiplication of signed magnitude data.
   b) Draw the flow chart for decimal division.

6. a) Draw and explain associative memory.
   b) How logical address mapping physical address? Explain with neat sketch.

7. a) How I/O Bus interconnected peripherals in computer?
   b) Draw block diagram of a typical asynchronous communication interface.

8. a) Outline the mutual exclusion with a semaphore in interprocessor communication and synchronization.
   b) Explain arithmetic pipeline with an example.

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Hall Ticket Number :										

R-11 / R-13

Code: 1G353

III B.Tech. I Semester Supplementary Examinations October 2020

Digital IC Applications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) Define logic levels, noise margins & write the importance of noise margins in different IC logic families.
   b) Design a CMOS logic circuit for Two input AOI gate and provide its functionality.

2. a) Explain the transistor switching operation of 2 input LS-TTL NAND with neat circuit diagram and truth tables.
   b) Distinguish between CMOS logic and TTL logic circuits.

3. a) Explain about various Data types used in VHDL.
   b) Describe the design flow diagram of VHDL.

4. a) With an example, mention the structural design elements of VHDL?
   b) Discuss any Three sequential statements with relevant examples.

5. a) Write short notes on three state devices.
   b) Explain about EX-OR gates and parity circuits with an example.

6. a) Write short notes on comparators.
   b) What is the purpose of Wait-statement in VHDL?

7. Draw and explain the logical operation of SR, JK, D, and T Flip-flops.

8. a) Write short notes on different ROMs and RAMs.
   b) Distinguish Static and Dynamic RAM.

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Hall Ticket Number :										

R-11 / R-13

Code: 1G352

III B.Tech. I Semester Supplementary Examinations October 2020

Linear IC Applications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1.	a)	Explain the operation of Differential Amplifier with neat block diagram.	7M
	b)	Why the Level Translator is called as an Emitter Follower and explain.	7M
2.	a)	Explain the operation of Op-Amp. in Inverting and Non-Inverting modes.	7M
	b)	List out the characteristics of Op-Amp. and explain.	7M
3.	a)	With neat sketch explain the working of practical differentiator and list the practical applications of a differentiator.	8M
	b)	Design a practical differentiator circuit to differentiate a signal of 4 Sin(400πt). Draw the input and output waveforms	6M
4.	a)	Explain how the precision rectifier is differ from the conventional rectifier.	6M
	b)	With neat sketch explain the working of full wave precision rectifier.	8M
5.	a)	What are the advantages of active filters over passive filters	7M
	b)	Design a first order butter worth band pass active filter with a pass band gain 4 and cut off frequencies 4 KHz- 8 KHz. Also obtain the response.	7M
6.	a)	Draw and explain the block schematic of IC565	7M
	b)	With neat sketch explain the frequency demodulation using PLL	7M
7.	a)	Explain about R-2R ladder DAC.	7M
	b)	Explain with a neat sketch the operation of Parallel Comparator.	7M
8.	a)	Explain in detail how Multipliers are classified.	7M
	b)	Explain the operation of Sample and Hold circuit in detail	7M

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