Hall	Ticł	xet Number :					
Code: 1G457							
III B.Tech. I Semester Supplementary Examinations November 2019							
Computer System Architecture							
Ma	x M	(Electronics and Communication Engineering) arks: 70	Time: 3 Hours				
TVIC.	A. 191	Answer any <b>five</b> questions	11110. 3 110013				
		All Questions carry equal marks ( <b>14 Marks</b> each)					
1.	a)	Describe with neat sketch the functional units of computers.	8M				
	b)	Explain in brief complements in data representation.	6M				
2.	a)	What is the need of three state buffers? Explain	7M				
	b)	Draw and describe flow chart for interrupt cycle.	7M				
3.		List and explain addressing modes.	14M				
4.	a)	Explain control memory with block diagram.	7M				
	b)	Draw the block diagram for selection of address for control memory	ory. 7M				
5.		With an example explain step-by-step procedure for division of tw binary numbers.	vo fixed-point 14M				
6.	a)	With neat sketch describe memory connection to CPU	7M				
	b)	How address mapping using pages in virtual memory?	7M				
7.	a)	Discus about Direct Memory Access.	7M				
	b)	Draw block diagram of a computer with I/O Processor. Describe.	7M				
8.	a)	Describe Crossbar switch interconnection structure.	7M				
	b)	Briefly explain the parallel processing. ***	7M				

Hall Tic	cket Number :								
R-11 / R-1									
Code: 1G353 III B.Tech. I Semester Supplementary Examinations November 2019									
Digital IC Applications									
(Electronics and Communication Engineering)									
Max. Marks: 70 Time: 3 Hours Answer any <b>five</b> questions									
	All Questions carry equal marks (14 Marks each)								
*****									
1. a)	Design a CMOS transistor circuit for a Two input XOR gate and explain the	71.4							
F.)	operation with the help of function table?	7M							
b)	Explain about CMOS steady electrical behavior in brief.	7M							
2. a)	Distinguish CMOS logic and TTL logic circuits.	6M							
b)	With the help of diagram explain the working of three input ECL-NOR gate.	8M							
3. a)	Describe the design flow of HDL with an example.	8M							
b)	Describe the program structure in VHDL.	6M							
4. a)	Distinguish concurrent and sequential signal assignment statements with an								
4. a)	example								
b)									
5. a)	Write a VHDL program for 4-bit grey to binary.	6M							
b)	Write a VHDL program for 3-8 decoder using case statement.	8M							
	Design 4 bit Perrol shifter and write a VHDL program for it	01/							
6. a)	Design 4-bit Barrel shifter and write a VHDL program for it.	8M GM							
b)	What is the purpose of Wait-statement in VHDL?	6M							
7. a)	Design Mod-7 counter using VHDL.	8M							
b)	Describe the importance of sensitivity list in a process statement.	6M							
8. a)	Distinguish Static and Dynamic RAM	6M							
b)	Describe the READ and WRITE operations of Dynamic RAM cell.	8M							
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Hall Ticket Number :												]				
Code: 1G352										J		J		R-	11 / F	R-13
	III B.Tech. I Semester Supplementary Examinations November 2019															
<b>Linear IC Applications</b> ( Electronics and Communication Engineering )																
Max	x. M	( El arks: 70	lectro	onic	cs ar	nd C	omr	nuni	cati	on E	ngir	ieeri	ng)		me: 3	Hours
					Ansv	ver d	any f	five	ques	stion	S					
All Questions carry equal marks ( <b>14 Marks</b> each)																
1.	<ol> <li>a) Explain the need for current mirror circuit with the help of circuit diagram.</li> <li>b) Discuss the DC analysis of Dual input balanced output configuration of differential amplifier.</li> </ol>							7M								
							on of a	a 7M								
2.	a)	Explain the bl	ock di	iaora	am re	pres	entat	ion o	fatv	pical	Op-/	Amp.				5M
	с)										9M					
0	,															
3.	a) b)	Draw and explain a differential amplifier with two Op-Amps. 7N														
	b)	Draw and explain the Op-Amp ideal integrator. Mention its drawbacks. How these are overcome with Lossy integrator?										7M				
4.	a)	What is the difference between a normal diode rectifier and a precision rectifier? Explain with neat diagrams.						? 7M								
	b) Design an Op-Amp Monostable multi for an output pulse duration of 1ms.						7M									
5.	a)	Design an Act	tive N	otch	filter	to re	ejecta	a frec	quenc	cy of	50 H	z.				8M
	b)	What are the Explain.	advar	ntag	es an	d dis	sadva	intag	es of	activ	e filt	ers o	ver p	bassive	e filters'	? 6M
6.	a)	Draw and explain the monostable operation of 555 timer. 7										7M				
	b)	Draw the block diagram of 565 PLL and explain its principle of operation. 7									7M					
7.	a)	Explain the v diagram.	vorkir	ng p	rincip	ole o	f sud	ccess	sive a	appro	oxima	ation	ADC	C with	a nea	it 7M
	b)	Explain the va	arious	DAG	C/AD	C sp	ecific	ation	s in c	letail						7M
8.	a)	Draw and exp	lain a	ı san	nple a	and h	nold c	ircuit	t.							7M
•	с, b)	Discuss the a			•											7M
	,		-				•	**								