Hall Ticket Number :										

R-14

Code: 4G351

III B.Tech. I Semester Supplementary Examinations May 2018

Control Systems

(Electronics and Communication Engineering)

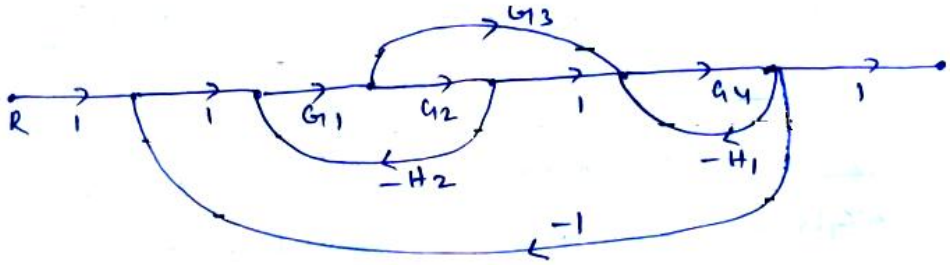
Max. Marks: 70 Time: 3 Hours

Answer all five units by choosing one question from each unit (5 x 14 = 70 Marks)

*****

UNIT–I

1. a) The signal flow graph for the system of figure is shown in below figure



7M

b) Compare the open loop and closed loop system with suitable examples 7M

OR

2. a) Explain the Mason's gain formula 7M

b) Obtain the transfer function of armature controlled DC motor 7M

UNIT–II

3. a) What are the time domain specifications 7M

b) Obtain the unit step response of a unity feedback system whose open loop transfer function is G(s) = $\frac{4}{s(s+5)}$ 7M

OR

4. Sketch the root locus plot of the control system with loop transfer function G(s)H(s)= $\frac{k}{s(s+4)(s^2+4s+8)}$ 14M

UNIT–III

5. Sketch the bode plot for the transfer function $\frac{300(s^2+2s+4)}{s(s+10)(s+20)}$ 14M

OR

6. a) Explain Nyquist criterion 7M

b) Explain how stability can be assessed from bode plots 7M

UNIT–IV

7. a) Explain the necessity of a compensator 7M

   b) Write the difference between lead and lag compensator 7M

OR

8. The open loop transfer function of the UFB system is $G(s) = \frac{k}{s(s+1)}$. It is desired to have the velocity constant K_v = 12 sec^{-1} and phase margin as 40 degrees. Design a lead compensator to meet the above specifications 14M

UNIT–V

9. a) Compute the STM for the system given the system matrix $A = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$ 7M

   b) Write the solution of linear state equations 7M

OR

10. a) Write short notes on controllability and observability 7M

    b) Check whether the system represented by

$$\dot{x} = \begin{bmatrix} -3 & 1 & 1 \\ -1 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix} x + \begin{bmatrix} 0 & 1 \\ 0 & 0 \\ 2 & 1 \end{bmatrix} u$$

$$y = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} x$$ observable (or) not 7M

***

Hall Ticket Number :										

R-14

Code: 4G455

III B.Tech. I Semester Supplementary Examinations May 2018

Computer System Architecture

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

****

UNIT–I

1. a) Explain the terms computer architecture, computer organization and computer design in a detailed fashion. 8M

   b) Discuss about fixed point and floating point representations. 6M

OR

2. a) Explain in brief about the performance of a computer system. 7M

   b) Discuss in detail about error detection codes. 7M

UNIT–II

3. a) Draw and explain the 4 bit binary adder-subtractor. 7M

   b) Explain in detail different computer instruction formats with examples. 7M

OR

4. a) Describe in brief various Logic Micro-operations. 7M

   b) Explain instruction cycle. How will you represent instruction cycle with interrupts? Explain. 7M

UNIT–III

5. a) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction 10M

   b) Explain the basis for booths multiplication algorithm along with its constituents Steps. 4M

OR

6. a) Hard wired control unit is faster than micro programmed control unit. Justify this statement 6M

   b) Explain with example the process of binary division in digital hardware. 8M

UNIT–IV

7. a) Explain the features of the cache memory and its accessing. 9M

   b) Explain in detail Isolated Vs Memory mapped I/O. 5M

OR

8. a) Explain in detail the virtual memory address translation. 9M

   b) Explain in detail I/O Bus Vs Memory Bus. 5M

UNIT–V

9. a) What is pipelining? Explain the arithmetic pipeline. 7M

   b) Explain in detail the system bus structure for multiprocessors. 7M

OR

10. a) Explain four segments pipelining with space time diagram. 7M

    b) Discuss in detail the characteristics of multiprocessors. 7M

***

Hall Ticket Number :										

R-14

Code: 4G353

III B.Tech. I Semester Supplementary Examinations May 2018

Digital IC Applications

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

****

UNIT–I

1. a) Define logic levels, noise margins & write the importance of noise margins in different IC logic families. 7M

   b) Design a CMOS transistor circuit for 3-input AOI gate and explain its operation. 7M

OR

2. a) List different types of logic families & compare with different parameters. 7M

   b) Draw and explain the circuit diagram of 2-input LS-TTL NAND gate. 7M

UNIT–II

3. a) Describe the design flow of HDL with an example. 8M

   b) Describe the program structure in VHDL. 6M

OR

4. Explain data objects , Functions and procedures of VHDL 14M

UNIT–III

5. a) Distinguish concurrent and signal assignment statement. 7M

   b) Design logic to detect prime number of a 4-bit input and write the VHDL code in data flow model. 7M

OR

6. a) Discuss any 3 sequential statements with an example each. 7M

   b) Explain delay models in VHDL. 7M

UNIT–IV

7. Draw pin diagram of IC 74X138 and write its VHDL code 14M

OR

8. Draw with neat sketch and explain Barrel shifter 14M

UNIT–V

9. a) Design universal shift register in VHDL 7M

   b) Write a VHDL code for SR flip flop in behavioral model. 7M

OR

10. a) Distinguish static and dynamic RAM 7M

    b) Describe the read and write operations of dynamic RAM cell. 7M

***

Hall Ticket Number :										

R-14

Code: 4G352

III B.Tech. I Semester Supplementary Examinations May 2018

Linear IC Applications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

****

UNIT–I

1. a) Derive the expressions for the dc operating point of dual input balanced output differential amplifier.

   b) With neat circuit diagram explain the operation of current mirror.

OR

2. With necessary circuits explain the techniques used to minimize offset voltage and offset current.

UNIT–II

3. a) Explain the operation of a three op-amp instrumentation amplifier.

   b) Design an op-amp differentiator that will differentiate an input signal with f_{max} = 100 Hz .

OR

4. a) Show that the pulse width of op-amp mono stable multi vibrator is T=0.69RC

   b) Describe the operation of a full wave rectifier with necessary waveforms

UNIT–III

5. Explain the astable multi vibrator operation of 555 timer and derive the expression for its duty cycle.

OR

6. a) With block diagram discuss the principle of operation of IC 565 PLL.

   b) How PLL is used as an AM detector?

UNIT–IV

7. Which is the fastest ADC? Explain the operation of (a) Successive approximation ADC (b) Flash ADC.

OR

8. a) What is the necessity of data conversion? Explain the working principle of R-2R ladder DAC.

   b) An 8-bit DAC has output voltage of 2.55V. Find its resolution.

UNIT–V

9. Mention the advantages of IC voltage regulators. With neat internal block diagram explain IC 723.

OR

10. a) Design a second order Butterworth LPF having upper cut-off frequency of 1KHz.

    b) Obtain transfer function and hence frequency response of a HPF.

***

Hall Ticket Number :										

Code: 4GA51

R-14

III B.Tech. I Semester Supplementary Examinations May 2018

Managerial Economics and Financial Analysis

(Common to CE, ME & ECE)

Max. Marks: 70 Time: 3 Hours

Answer all five units by choosing one question from each unit (5 x 14 = 70 Marks)

*****

UNIT-I

1. Define Price elasticity, Income elasticity and Cross price elasticity of demand. What are the different methods of measuring Price Elasticity of demand? Derive relationship between Price Elasticity of Demand and Marginal Revenue?

OR

2. Define Managerial Economics. Discuss the nature and scope of Managerial Economics. What is the relationship of Managerial Economics with Microeconomics?

UNIT-II

3. What is the shape of long-run average cost curve and explain why? Differentiate between Economies of Scale and Economies of Scope with suitable examples.

OR

4. Define and show graphically the Break even point of a firm. Find out the break even output (Q*) of a firm if total cost (TC) = Rs. 6310; total revenue (TR) = Rs. 4130; fixed cost (FC) = Rs. 4980; variable cost (VC) = Rs. 1330 and present output (Q) = 5.

UNIT-III

5. Compare and Contrast the Short-run and Long-run equilibrium conditions under Perfect competition and Monopoly market.

OR

6. Define Oligopoly market structure. Describe how price and output is determined under Stackelberg Duopoly model.

UNIT-IV

7. Why is capital important for a firm? What are the various sources of raising capital? Elaborate.

OR

8. What is capital budgeting? Define Net Present Value and Discount Rate. Write a brief note on Pay Back Method.

UNIT-V

9. What do you understand by the term ‘Ledger’ and ‘Trial Balance’? Name two methods of preparing a Trial Balance. Prepare a purchase book from the following information:
   a) Purchase of goods costing Rs. 5000/- from M/s Ramesh & Co. vide invoice no. 120 dated 15/09/2017.
   b) Purchase of Fixed Assets costing Rs. 8000/- from M/s Renu & Co. vide invoice no. 016 dated 20/09/2017.
   c) Paid wages of Rs. 600/- in cash vide receipt no.16 dated 25/09/2017.

OR

10. What is the meaning of Accounting Ratios? What are the objectives of ratio analysis? List out the advantages and limitations of ratio analysis.

***