Hall Ticket Number :

R-15

Code: 5G354

III B.Tech. I Semester Supplementary Examinations May 2019
Antennas and Wave Propagation
(Electronics and Communication Engineering)

Max. Marks: 70   Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)
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UNIT–I

1. a) What is the effective aperture of an Antenna and how it related to the gain?   7M

    b) Discuss the effect of ground on the Radiation Patterns of Vertical and Horizontal Dipoles.   7M

OR

2. What is meant by Directivity and Power gain of an Antenna? Show how the Directivity can be increased by using a number of Antennas in a suitable Array.   14M

UNIT–II

3. What are antenna arrays why they are used in practice? Obtain the expression for the array of 3-element linear array, if all the 3-elements are excited equally and in-phase, in which Direction would the major lobe point.   14M

OR

4. a) Explain the principle of Pattern multiplication and find the array factor of a two element array.   7M

    b) Write short notes on synthesis of specified Azimuthal pattern.   7M

UNIT–III

5. Explain the important features of the Horn antenna and the principle of its working. How the Antenna fed and what are its applications.   14M

OR

6. With neat diagram explain the working principle of Lens antennas.   14M

UNIT–IV

7. a) Discuss the effects of earth properties on Ground wave Propagation.   7M

    b) Write short notes on space wave and sky wave propagation.   7M

OR

8. Discuss the mechanism of medium wave propagation through atmosphere .what are the effects of refraction in the atmosphere and earths curvature in the medium wave propagation.   14M

UNIT–V

9. a) Obtain the expression for range of Lion-of-Sight for space wave propagation in terms of antennas transmitting receiving heights.   7M

    b) Find the range of LOS system when they receive and transmit antenna heights are 10m and 100m respectively. Take the effective earth's radius into consideration.   7M

OR

10. Describe the structure of atmosphere .Discuss briefly the part played by the ionosphere in radio wave propagation.   14M

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III B.Tech. I Semester Supplementary Examinations May 2019
Control Systems
(Electronics and Communication Engineering)

Max. Marks: 70   Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) What are the assumption are made to determine the transfer function of DC servo motor in field control method?   4M

   b) Write differential equations of the following mechanical system and find Transfer Function Y(s)/F(s).
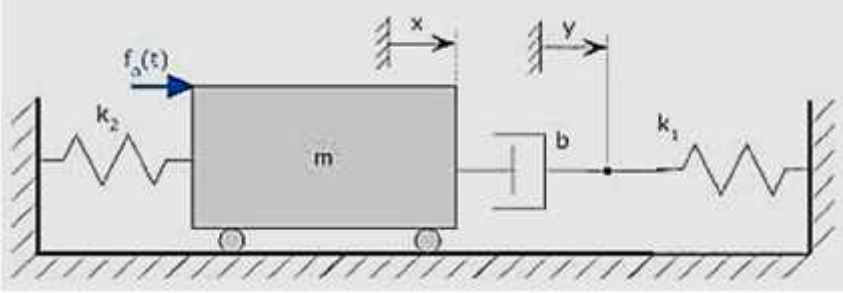
     10M

OR

2. a) State the rule for shifting the summing point right and left side of the block.   3M

   b) For given block diagram as shown in figure, find the transfer function C(s)/R(s).
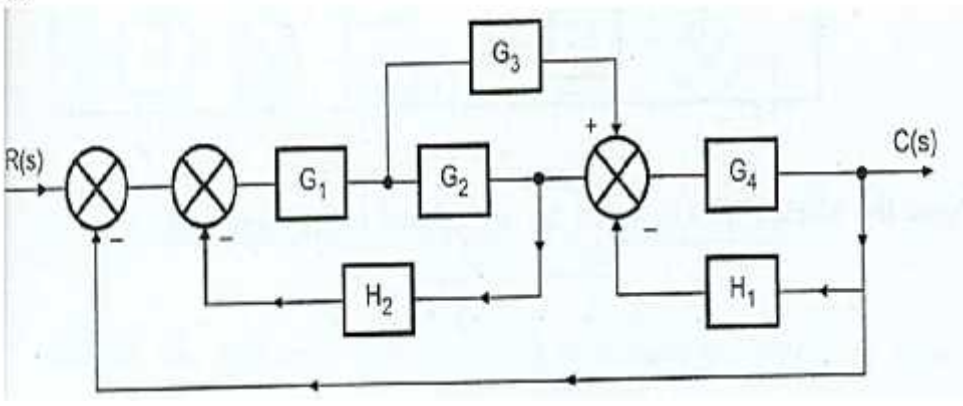
     11M

UNIT–II

3. a) Explain TYPE and ORDER of a system.   4M

   b) Derive the expression for transient specifications Rise Time, Peak time and settling time.   10M

OR

4. A unity feedback control system with $G(S)H(S) = \dfrac{K}{S(1+0.1S)(1+0.2S)}$

   a) Sketch the root locus diagram of the system   9M

   b) Determine the limiting value of gain K for stability.   5M

UNIT–III

5. a) The open loop transfer function of a unity feedback system is given by
$G(s) = \dfrac{1}{s(1+s)^2}$. Sketch the polar plot and determine the gain and phase
margin.   10M

   b) What are the advantages of polar plot over the bode plot.   4M

OR

6. a) The damping ratio and natural frequency of oscillation of a second order system is 0.5 and 8 rad/sec respectively. Calculate
   i. Resonant peak.
   ii. Resonant frequency.
   iii. Band Width.   7M

   b) Explain the process of determination of Gain margin and Phase margin from polar plot.   7M

UNIT–IV

7. a) Explain with example the procedure for designing Lead Compensator.   9M

   b) Describe the effects and limitations of lag compensator.   5M

OR

8. a) Explain with example the procedure for designing Lag Compensator.   8M

   b) Compare the characteristics of three types of compensators.   6M

UNIT–V

9. a) Find the state transition matrix for $A = \begin{bmatrix} 0 & -1 \\ 2 & -3 \end{bmatrix}$
                                                                                                 9M

   b) What are the advantages of State space analysis?   5M

OR

10. a) Write the Properties of State Transition Matrix.   6M

   b) Obtain the state model of given electrical system.

                                                                                                 8M
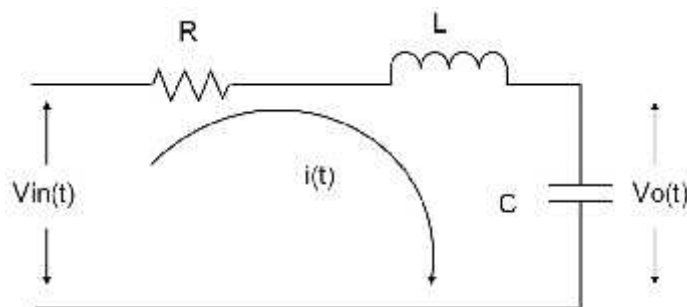
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III B.Tech. I Semester Supplementary Examinations May 2019
Computer System Architecture
(Electronics and Communication Engineering)

Max. Marks: 70   Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. Derive an algorithm in flowchart form for adding and subtracting two fixed-point binary numbers when negative numbers are in signed-l's complement representation.   14M

OR

2. a) Explain the functionalities of a computer.   7M

    b) Perform the arithmetic operations (+42) + (- 13) and (-42) - (- 13) in binary using signed-2's complement representation for negative numbers.   7M

UNIT–II

3. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?   14M

OR

4. a) What are the two instructions needed in the basic computer in order to set the E flip-flop to 1?   7M

    b) Design a 4-bit combinational circuit decrementer using four full-adder circuits.   7M

UNIT–III

5. a) Explain Multiplication algorithm with example.   7M

    b) List and Explain about Addressing modes.   7M

OR

6. a) What must the address field of an indexed addressing mode instruction be to make it the same as a register indirect mode instruction?   7M

    b) Explain about Instruction formats.   7M

UNIT–IV

7. a) Draw and Explain about Block Diagram and Functional Table of Main Memory   7M

    b) Explain various mapping procedures of cache memory with an example.   7M

OR

8. a) Explain briefly about Serial Communication.   7M

    b) List and explain about the registers, which are used in asynchronous communication interface.   7M

UNIT–V

9. a) What is Array Processor and explain with example.   7M

    b) Explain about Arithmetic pipeline.   7M

OR

10. a) Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization and Programming techniques.   7M

    b) Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment.   7M

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III B.Tech. I Semester Supplementary Examinations May 2019
Digital Communication
(Electronics and Communication Engineering)

Max. Marks: 70   Time: 3 Hours
Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)
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UNIT–I

1 a) Obtain the expression for quantization noise power in PCM system   6M
   b) With a neat sketch explain the operation of differential PCM (DPCM) system   8M

OR

2 a) Explain the working of delta modulation system with neat block diagram   8M
   b) A delta modulation system is designed to operate at three times the nyquist
      rate for a signal with a 3 KHz bandwidth. The quantization step size is 250 mV.
      Determine the maximum amplitude of a 1 KHz input sinusoid for which the delta
      modulation system does not have slope overload distortion   6M

UNIT–II

3 a) Write a brief note on baseband signal receiver   4M
   b) Derive an expression for error probability of optimum filter   10M

OR

4 a) Obtain the expression for impulse response of matched filter   8M
   b) Illustrate the principle and operation of correlator   6M

UNIT–III

5 a) Explain the transmitter and receiver sections of BPSK scheme   8M
   b) Discuss about non-coherent detection of BFSK waves   6M

OR

6 a) Draw and explain the transmitter and receiver sections of M-ary FSK scheme   8M
   b) Compare the transmission power, bandwidth and bit error rate parameters of
      various digital modulation techniques   6M

UNIT–IV

7 a) Define and explain the following:
      (i) Self information   (ii) Average information
      (iii) Information rate   (iv) Mutual information   14M

OR

8 a) Explain the implications of Shannon-Hartley theorem   6M
   b) Construct the Huffman code for the word **COMMITTEE**   8M

UNIT–V

9 a) Describe the matrix representation of linear block codes   6M
   b) Design an encoder for the (7, 4) binary systematic cyclic code generated by
      $g(x) = x^3+x+1$ and verify its operation using message: 0101   8M

OR

10 a) Explain the operation of convolutional code generation by using an appropriate
      shift register and modulo-2 adder configurations   8M
   b) Write a brief note on BCH codes   6M

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Code: 5GA51

III B.Tech. I Semester Supplementary Examinations May 2019
Managerial Economics and Financial Analysis
(Common to CE, ME and ECE)

Max. Marks: 70   Time: 3 Hours
Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)
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UNIT–I

1.   What do you understand by elasticity of demand? How do you measure its. What is its significance?

OR

2.   Write elasticity demand and factors governing elasticity of demand.

UNIT–II

3.   State the break even analysis? Explain objectives, importance and show the graphical representation of BEP.

OR

4.   Rainbow enterprises deals in the supply of computers the following cost data available for two successive periods

	Year 1 Rs	Year 2 Rs
sales	50000	120000
Fixed costs	10000	20000
Variable cost	30000	60000

determine

    a) p/v ratio   4 marks
    b) breakeven point   5 marks
    c) margin of safety   5 marks

UNIT–III

5.   Elaborate monopoly market and price out-put determination in short run and long run.

OR

6. a) What are the causes for the emergence of monopoly?

    b) How is the equilibrium position attained by monopoly list under varying cost conditions?

UNIT–IV

7.   What is working capital? Explain the factors governing working capital requirements?

OR

8.   A business firm is thinking of choosing the right machines for their purpose after financial evolution of the proposals the initial cost and the net cash flow over five years to the business firm have been calculated for each machine as follows.

	Machine 1 (Rs)	Machine 2 (RS)
Initial cost	20000	28000
annual cash inflow 1year	8000	10000
2 year	12000	12000
3 year	9000	12000
4 year	7000	9000
5 year	6000	9000

Choose the machine based on i) payback period ii) accounting rate return

UNIT–V

9. From the following trial balance of xyz ltd prepare trading and profit&loss account for the year ending 31-3-2017 and balance sheet as on date considering the adjustments given below:

Debit balances	Rs	Credit balances	Rs
buildings	70000	Carriage in wards	1291
Motor trucks	12000	Reserve doubtful debts	1320
furniture	1640	Establishments expenses	2135
debtors	15600	Carriage out wards	800
creditors	18852	insurance	783
stock	15040	interest	340
Cash in hand	988	bad debts	613
Cash at bank	14534	Audit fee	400
Bills receivables	5844	General expenses	3050
purchases	85522	investments	8922
discount	945	sales	121850
Returns in word	285	capital	920000
		Bills payable	6930
		rent	900

Adjustments: 1) closing stock Rs 15000 2) depreciation on motor trucks 20% and furniture 10% per annum 3)write of bad debts of Rs100 and maintain at 5% reserve for doubtful   debts 4) prepaid insurances Rs 150   5)interest accrued but not received Rs 120

OR

10. Write Short notes on
   a) Liquidity ratios   3M
   b) Profitability ratios   4M
   c) Activity ratios   4M
   d) Capital structure ratios are illustrating suitable example. 3M

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III B.Tech. I Semester Supplementary Examinations May 2019
Analog & Digital Integrated Circuits
(Electronics and Communication Engineering)

Max. Marks: 70   Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. Draw the circuit of inverting and non-inverting amplifiers using Op-Amp and derive an expression for their gain   14M

OR

2. a) Discuss the operation of multiplier and divider   8M

    b) What are the merits and demerits of above   6M

UNIT–II

3. Explain the Astable and Monostable Multivibrator using Op-Amp with a neat diagram   14M

OR

4. a) Discuss in detail about successive approximation type DAC   8M

    b) What are the applications of PLL   6M

UNIT–III

5. a) Discuss the CMOS Dynamic Electrical Behavior   8M

    b) Give some advantages and disadvantages of above   6M

OR

6. Design the Operation of Universal Gate with ECL technology   14M

UNIT–IV

7. Explain the operation of BCD to Seven Segment decoder display using VHDL case statement   14M

OR

8. Discuss the Entities, Architectures and Configurations of VHDL design with an example.   14M

UNIT–V

9. Write a VHDL entity and architecture for a 3-bit synchronous counter using flip flops   14M

OR

10. Explain the operation of T-flip flop and JK flip-flop with VHDL code.   14M

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