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R-15

Code: 5G152

III B.Tech. I Semester Supplementary Examinations October 2020

Computer Networks

(Common to CSE & IT)

Max. Marks: 70

Time: 3 Hours

Answer all five units by choosing one question from each unit (5 x 14 = 70 Marks)

UNIT-I

- 1. a) Illustrate the functionality of various layers present in OSI model with a neat sketch. 10M
- b) List any two reasons for layered protocols and what is one possible disadvantage for Layered protocols? 4M

OR

- 2. a) Briefly explain the following 8M
 - i). Twisted pair cable. ii). Co-Axial cable iii). Fiber optic cable
- b) Explain the Structure of Telephone networks. 6M

UNIT-II

- 3. a) Write short notes on different Framing methods in Data Link Layer. 8M
- b) Explain about Stop and Wait protocol. 6M

OR

- 4. a) Discuss about the Wireless LAN MAC protocols. 8M
- b) Draw and Explain IEEE 802.11 data frame format. 6M

UNIT-III

- 5. a) Describe the major differences between the ECN method and the RED method of congestive avoidance. 5M
- b) Explain in detail about the Link State Routing Algorithm with an example 9M

OR

- 6. a) What is a Routing protocol? List and explain the principles of routing 9M
- b) Convert the IP address whose hexadecimal representation is C22F1582 to dotted decimal notation. 5M

UNIT-IV

- 7. Explain the following transport layer protocols. 14M
 - a) Simple protocol b) Stop and wait protocol
 - c) Go-Back-N protocol d) Selective Repeat Protocol

OR

- 8. a) Draw TCP header format. Write the significance of the components in TCP header format 9M
- b) Discuss the advantages and disadvantages of Delay Tolerant Networks 5M

UNIT-V

- 9. Explain about Domain Name System and its advantages. 14M

OR

- 10. a) Write short notes on Real time conferencing. 7M
- b) Write short notes on Content Delivery Networks. 7M

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R-15

Code: 5G356

III B.Tech. I Semester Supplementary Examinations October 2020

Micro Processors and Interfacing

(Common to CSE & IT)

Max. Marks: 70

Time: 3 Hours

Answer all five units by choosing one question from each unit (5 x 14 = 70 Marks)

UNIT-I

- 1. a) Discuss the functions of BIU & EU in 8086. 9M
- b) List out features of 8086 microprocessor. 5M

OR

- 2. a) Describe the flag register of 8086. 7M
- b) Discuss how physical address is generated in 8086? 7M

UNIT-II

- 3. a) Draw the basic structure of SRAM and DRAM cells 5M
- b) Construct an interface of two 4K X 8 EPROMS & two 4K X 8 RAM chips with 8086. Select suitable memory map. 9M

OR

- 4. a) Explain the interfacing diagram of ADC with 8255. 7M
- b) Explain how a stepper motor is interfaced to 8086. 7M

UNIT-III

- 5. a) Draw the architecture of 8257. Explain about it. 7M
- b) What are the differences between Programmed I/O and Interrupt driven I/O. 7M

OR

- 6. a) Explain the interrupt response of 8259. 7M
- b) Draw the interrupt vector table. 7M

UNIT-IV

- 7. a) Name serial communication standards and draw TTL to RS232 and RS232 to TTL conversion. 7M
- b) Explain 8251 USART architecture. 7M

OR

- 8. a) Explain different modes of operation of 8253/54. 7M
- b) Differentiate between Asynchronous and Synchronous data transfer schemes. 7M

UNIT-V

- 9. a) What are the difference between logical address, linear address and physical address? 8M
- b) Explain the salient features of 80386. 6M

OR

- 10. a) Explain descriptor tables of 80286 and 80386 processor 7M
- b) What do you mean by paging? What are its advantage and disadvantage? 7M

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R-15

Code: 5G455

III B.Tech. I Semester Supplementary Examinations October 2020

Software Testing Methodologies

(Information Technology)

Max. Marks: 70

Time: 3 Hours

Answer all five units by choosing one question from each unit (5 x 14 = 70 Marks)

UNIT-I

- 1. a) Explain Purpose of testing 7M
- b) Briefly define how to model for testing 7M

OR

- 2. a) Explain various consequences of bugs 7M
- b) Explain taxonomy of bugs 7M

UNIT-II

- 3. What is meant by statement coverage(C1) and branch coverage(C2), explain with an example how to select enough paths to achieve (c1+c2) 14M

OR

- 4. Write short notes on
- a) Predicate and path Predicate
- b) Path instrumentation 14M

UNIT-III

- 5. Discuss about transaction flow testing techniques 14M

OR

- 6. What are the different properties of nice domain, why these properties are important in domain testing explain them 14M

UNIT-IV

- 7. a) Explain Path products 7M
- b) Explain path expression 7M

OR

- 8. What are regular expressions and define various types in it 14M

UNIT-V

- 9. a) Differentiate between good state graph and bad graph state graph 7M
- b) Explain the purpose of state testing 7M

OR

- 10. What are the partial ordering relations explain them with example 14M
