# Hall Ticket Number : 

$\square$

## Code: 7G353

## R-17

III B.Tech. I Semester Supplementary Examinations March/April 2023

## Analog \& Digital Integrated Circuits Applications

(Electronics and Communication Engineering)
Max. Marks: 70
Time: 3 Hours
Answer any five full questions by choosing one question from each unit ( $5 \times 14=70$ Marks )
$* * * * * * * * *$

## UNIT-I

1. Discuss about Inverting \& Non- Inverting Op-Amp circuits and derive the expression for the gain.

## OR

2. Discuss the characteristics of instrumentation amplifier with the circuit and derive the expression of voltage gain.

## UNIT-II

3. Explain the operation of mono stable multi vibrator using 555 timers and derive the expression of time delay

## OR

4. a) Discuss about advantages and disadvantages of Flash ADC over successive approximation type ADC
b) Summarize the working principle of R-2R ladder DAC
$6 \mathrm{M} \mathrm{CO1} \mathrm{~L} 2$
8M CO1 L2

## UNIT-III

5. Analyze the working of CMOS Inverter and its characteristics.

OR
6. Discuss about the CMOS Dynamic Electrical Behavior.

UNIT-IV
7. Explain with neat structure of $8 \times 3$ encoder with the VHDL program for standard IC $74 \times 148$.

14 M CO 3

## OR

8. a) List out the advantages of Combinational Circuits

6M CO2 L1
b) Design Full adder using half adders.

## UNIT-V

9. Apply VHDL methodology to D flip-flop and SR flip-flop. 14M CO3 L3
OR
10. a) Evaluate the Characteristic equations of SR and JK Flip-Flops.

7M CO3 L5
b) Solve JK flip-flop into D Flip-Flop.

