Hall Ticket Number :										

R-17

Code: 7G352

III B.Tech. I Semester Supplementary Examinations June 2022

Control Systems

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *any five full questions* by choosing one question from each unit (5x14 = 70 Marks)

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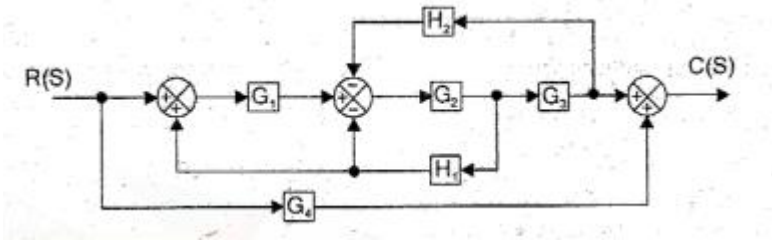
Marks

UNIT–I

1. a) List out the advantages and drawbacks of open loop[and closed loop control systems 7M
   b) Explain the feedback characteristics of closed loop control system 7M

OR

2. a) Determine the closed loop transfer function C(s)/R(s) of the system as shown figurer below 10M



   b) Classify the types of control systems 4M

UNIT–II

3. a) Discuss about procedural steps to sketch root locus 7M
   b) Find the breakaway point and angle of departure of a unity feedback system has open loop transfer function G(s)= K/s(s^2+4s=13) 7M

OR

4. Obtain the steady state error e_{ss} of Type-0, Type-1 and Type-2 systems for unit step, ramp and parabolic inputs 14M

UNIT–III

5. a) Explain about frequency domain specifications 7M
   b) Describe the procedure for developing the polar plot 7M

OR

6. Define the following terms 14M
   (i) Gain cross over frequency (ii)Phase cross over frequency
   (iii) Gain margin (iv)Phase margin

UNIT–IV

7. a) Discuss about controllers. Explain about different types of controllers 7M
   b) Discuss the design procedure of PID controller 7M

OR

8. a) Distinguish the lead and lag compensators 7M
   b) Calculate the transfer function of lead compensator 7M

UNIT–V

9. a) Discuss the significance of state space analysis 7M
   b) Define the terms controllability and observability and write necessary conditions for verification of controllability and observability 7M

OR

10. Define (i) state (ii) state variables (iii) state space representation 14M

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III B.Tech. I Semester Supplementary Examinations June 2022

Analog & Digital Integrated Circuits Applications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *any five full questions* by choosing one question from each unit (5x14 = 70 Marks)

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			Marks
		UNIT–I	
1.		Discuss the operation of Op-Amp block diagram and its characteristics	14M
		OR	
2.	a)	Identify the applications of Op-amp and its advantages.	7M
	b)	List out the characteristics of Ideal Op-amp.	7M
		UNIT–II	
3.	a)	Explain the functional diagram of IC 555 with a neat sketches	8M
	b)	List out the applications of PLL	6M
		OR	
4.	a)	Restate the operation of Zero Cross Detector and Window Detector	7M
	b)	Analyze the basic principle of successive approximation type ADC	7M
		UNIT–III	
5.	a)	Design 2-input NOR gate using CMOS Logic.	7M
	b)	Differentiate between CMOS and TTL families.	7M
		OR	
6.		Summarize the steady state electrical behavior of CMOS circuits	14M
		UNIT–IV	
7.	a)	Design Full adder using half adders.	8M
	b)	Discuss about logic gates used Combinational Circuits	6M
		OR	
8.		Define decoder and explain with neat diagram the functionality of 3 to 8 decoder also write the VHDL program for standard 74X138.	14M
		UNIT–V	
9.	a)	Differentiate between latches and Flip-Flops.	7M
	b)	Evaluate the Characteristic equations of SR and JK Flip-Flops.	7M
		OR	
10.		Design 3-bit SISO Shift register using Flip-Flops.	14M

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