| Hall Ticket Number : | | | | | | | | | | |
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**R-20**

**Code: 20A45DT**

III B.Tech. I Semester Supplementary Examinations June 2024

# Pulse and Digital Circuits

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. In Part-A, each question carries **Two marks.**
3. Answer **ALL** the questions in **Part-A** and **Part-B**

## PART-A

**( Compulsory question )**

| | | CO | BL |
|---|---|---|---|
| 1. Answer ***all*** the following short answer questions ( 5 X 2 = 10M ) | | | |
| a) | Define the term rise time and write its expression. | 1 | 1 |
| b) | What is meant by clipper and list out the various types? | 1 | 1 |
| c) | Define the types of states in multi vibrators. | 2 | 1 |
| d) | Briefly discuss about the Commutating Capacitors? | 2 | 1 |
| e) | Differentiate between logic gates and sampling gates | 4 | 4 |

## PART-B

**Answer *five* questions by choosing one question from each unit ( 5 x 12 = 60 Marks )**

| | | | Marks | CO | BL |
|---|---|---|---|---|---|
| | | **UNIT-I** | | | |
| 2. | a) | Find the response of a High Pass RC Circuit for Symmetrical Square wave input. Also, derive the expression of percentage tilt | 6M | 1 | 4 |
| | b) | Explain how an RC high pass circuit acts as a differentiator | 6M | 1 | 2 |
| | | **OR** | | | |
| 3. | a) | Analyze the response of a low pass RC circuit for the Pulse input signal | 6M | 1 | 4 |
| | b) | Show that how RC low pass circuit acts as an integrator | 6M | 1 | 3 |
| | | **UNIT-II** | | | |
| 4. | a) | Draw the circuit diagram for positive clamper circuit and explain its principle of operation. | 6M | 2 | 1 |
| | b) | Discuss the function of series diode and shunt diode clipping circuits? How can the clipping level shifted to reference voltage? Explain? | 6M | 2 | 2 |
| | | **OR** | | | |
| 5. | a) | Explain the working of transistor clipper. | 5M | 2 | 2 |
| | b) | With neat circuit diagram, explain the working of an emitter coupled clipper. | 7M | 2 | 1 |
| | | **UNIT-III** | | | |
| 6. | a) | Derive the expression for frequency of oscillation of an Astable multi vibrator. | 6M | 2 | 5 |
| | b) | With the help of neat circuit diagram explain Monostable Multivibrator and derive an expression for pulse width. | 6M | 2 | 2 |
| | | **OR** | | | |
| 7. | | Design and explain the operation of Schmitt trigger circuit and derive the expressions for UTP and LTP | 12M | 2 | 6 |
| | | **UNIT-IV** | | | |
| 8. | a) | Explain the working of transistor based Bootstrap time base generator circuit, and draw the necessary waveforms. | 6M | 3 | 1 |

| | | | | | |
|---|---|---|---|---|---|
| | b) | Draw and clearly indicate the restoration time and flyback time on the typical waveform of a time base voltage. | 6M | 3 | 2 |
| | | **OR** | | | |
| 9. | a) | Explain the working principle of UJT sweep circuit. | 6M | 3 | 3 |
| | b) | Explain the working principle of Boot-strap –time base generator. | 6M | 3 | 1 |
| | | **UNIT-V** | | | |
| 10. | a) | What is sampling Gate? And explain the basic operating principle of gates? | 6M | 4 | 2 |
| | b) | Explain the operation of unidirectional diode gate | 6M | 4 | 2 |
| | | **OR** | | | |
| 11. | a) | Classify the different logic systems and explain in detail | 6M | 4 | 2 |
| | b) | Design and verify the truth table of two input DTL NAND gate with the circuit diagram | 6M | 4 | 6 |

*** End ***

| Hall Ticket Number : | | | | | | | | | | |
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**R-20**

**Code: 20A451T**

III B.Tech. I Semester Supplementary Examinations June 2024

# VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. In Part-A, each question carries **Two marks.**
3. Answer **ALL** the questions in **Part-A** and **Part-B**

## PART-A

**( Compulsory question )**

| 1. Answer ***all*** the following short answer questions ( 5 X 2 = 10M ) | CO | BL |
|---|---|---|
| a) List the basic process for IC fabrication | 1 | 4 |
| b) Mention the different NOS Layers and draw their layout encodings | 2 | 1 |
| c) Give the name of different alternative gate circuits | 3 | 1 |
| d) Draw the basic structure of a dynamic CMOS gate? | 4 | 1 |
| e) What is the need for Testing? | 5 | 1 |

## PART-B

**Answer *five* questions by choosing one question from each unit ( 5 x 12 = 60 Marks )**

| | | | Marks | CO | BL |
|---|---|---|---|---|---|
| | | **UNIT-I** | | | |
| 2. | a) | List out the steps involved in the VLSI Design Flow and explain | 12M | 1 | 1 |
| | b) | Draw and explain the operation of BICMOS inverter circuit | 2M | 1 | 2 |
| | | **OR** | | | |
| 3. | a) | Derive the Ids – Vds relationship of MOS transistor in non-saturated and saturated region | 6M | 2 | 6 |
| | b) | With neat sketches explain PMOS fabrication | 6M | 2 | 2 |
| | | **UNIT-II** | | | |
| 4. | a) | Derive the expression for resistance estimation in VLSI circuits. | 6M | 2 | 3 |
| | b) | Write short notes on driving large capacitive loads. | 6M | 2 | 2 |
| | | **OR** | | | |
| 5. | a) | Explain the 2μm CMOS design rules for contacts and transistors. | 6M | 2 | 2 |
| | b) | Briefly discuss about scaling of MOS circuits and its limitations | 6M | 2 | 4 |
| | | **UNIT-III** | | | |
| 6. | a) | Explain different switch logic used for designing of VLSI circuits? | 6M | 4 | 2 |
| | b) | Derive an expression for sheet resistance (Rs) and apply the concept for calculation of sheet resistance for CMOS inverter. | 6M | 4 | 6 |
| | | **OR** | | | |
| 7. | a) | Write short notes on sheet Resistance and Wiring capacitances | 6M | 4 | 1 |
| | b) | Calculate inverter resistance for nMOS with Zpu=8 for pull up transistor and Zpd=1for pull down transistor and for CMOS Zpu=1 for pull up transistor and Zpd=1 for pull down transistor. | 6M | 4 | 3 |
| | | **UNIT-IV** | | | |
| 8. | a) | Describe the nature of a parity generator and explain its structured design approach. | 6M | 4 | 2 |
| | b) | Explain in detail about design flow of FPGA. | 6M | 4 | 2 |

**OR**

| | | | | | |
|---|---|---|---|---|---|
| 9. | a) | Give the subsystem design considerations of a four-bit adder | 6M | 4 | 4 |
| | b) | Explain step-by-step subsystem design approach. Consider an example. | 6M | 4 | 2 |

**UNIT-V**

| | | | | | |
|---|---|---|---|---|---|
| 10. | a) | Explain the concept of design verification and design capture tools used in VHDL synthesis. | 9M | 5 | 2 |
| | b) | Discuss about the Layout design for improved testability? | 3M | 5 | 2 |

**OR**

| | | | | | |
|---|---|---|---|---|---|
| 11. | a) | What is testing? What is the role of testing in VLSI Design? | 5M | 5 | 1 |
| | b) | Describe briefly about chip level test techniques | 7M | 5 | 3 |

*** End ***

| Hall Ticket Number : | | | | | | | | | | |
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**R-20**

**Code: 20A452T**

III B.Tech. I Semester Supplementary Examinations June 2024

## Control Systems

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. In Part-A, each question carries **Two marks.**
3. Answer **ALL** the questions in **Part-A** and **Part-B**

### PART-A

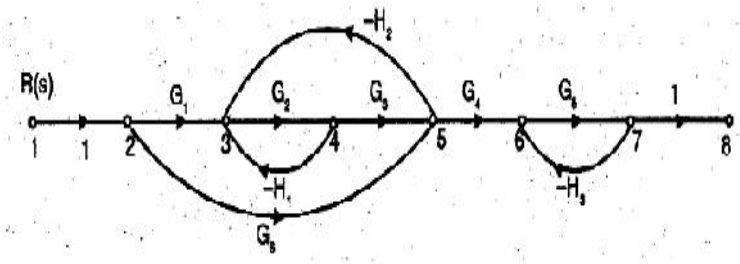
**(Compulsory question)**

| | | CO | BL |
|---|---|---|---|
| 1. | Answer ***all*** the following short answer question (5 X 2 =10M ) | | |
| a) | Define open loop and closed loop control system by giving suitable examples. | CO1 | L1 |
| b) | Define Peak over shoot | CO2 | L3 |
| c) | Explain about phase margin and gain margin | CO3 | L2 |
| d) | What are M and N circles? | CO4 | L2 |
| e) | Define State Transition Matrix | CO5 | L1 |

### PART-B

**Answer *five* questions by choosing one question from each unit ( 5 x 12 = 60 Marks )**

| | | Marks | CO | BL |
|---|---|---|---|---|
| | **UNIT–I** | | | |
| 2. a) | Classify various types of control systems | 4M | CO1 | L1 |
| b) | Find the transfer function of signal flow graph given below by using mason's gain formula | | | |




8M CO1 L3

**OR**

| | | | | |
|---|---|---|---|---|
| 3. | Derive an expression for the transfer function of an armature controlled DC servo motor | 12M | CO1 | L3 |
| | **UNIT–II** | | | |
| 4. | Determine the stability of the system whose characteristic equation is $3s^4+10s^3+5s^2+5s+2=0$, using Routh stability criterion. | 12M | CO2 | L5 |

**OR**

5. By means of RH criterion determine the stability of the system represented by the characteristic equation

$$S^4+2S^3+8S^2+4S+3=0$$ 12M CO2 L3

**UNIT–III**

6. a) Discuss the advantages of the Bode plot technique. 6M CO3 L2

   b) Distinguish between gain margin and phase margin 6M CO3 L2

**OR**

7. A certain system transfer function is

$$G(s)H(s)=\frac{75(1+0.2s)}{s(s^2+16s+100)}$$

using Bode plots, find gain margin and phase margin. Comment on stability. 12M CO3 L3

**UNIT–IV**

8. Explain the different steps to be followed for the design of lead-lag compensator using Bode plot. 12M CO4 L2

**OR**

9. a) Distinguish the P,D and I controllers 6M CO1 L3

   b) Determine the transfer function lag compensator 6M CO2 L3

**UNIT–V**

10. a) Discuss about the properties of the state transition matrix 4M CO1 L2

    b) Find the state transition matrix for

$$\dot{X}=\begin{bmatrix}-2 & 1 & 0\\ 0 & -2 & 1\\ 0 & 0 & -2\end{bmatrix}x.$$ 8M CO3 L3

**OR**

11. Develop the state vector x(t) for the state model

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix}=\begin{bmatrix}-12 & 2/3\\ -36 & -1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}1/3\\ 1\end{bmatrix}u;$$

And the initial conditions are $X_1(0)=2$, $X_2(0)=1$ 12M CO3 L3

*** End ***

| Hall Ticket Number : | | | | | | | | | | |
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**R-20**

**Code: 20A25FT**

III B.Tech. I Semester Supplementary Examinations June 2024

# Electric Vehicles

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**

2. In Part-A, each question carries **Two marks.**

3. Answer **ALL** the questions in **Part-A** and **Part-B**

## PART-A

**(Compulsory question)**

| | | CO | BL |
|---|---|---|---|
| 1. | Answer ***all*** the following short answer questions ( 5 X 2 = 10M ) | | |
| a) | What is the need and importance of electric vehicle? | CO1 | L2 |
| b) | Mention the importance of electric vehicles. | CO2 | L1 |
| c) | Define fuel cells. | CO3 | L2 |
| d) | What are the main components of an EV battery? | CO4 | L1 |
| e) | List any four application of the fuel cells? | CO5 | L2 |

## PART-B

**Answer *five* questions by choosing one question from each unit ( 5 x 12 = 60 Marks )**

| | | | Marks | CO | BL |
|---|---|---|---|---|---|
| | | **UNIT-I** | | | |
| 2. | a) | Explain about the history of hybrid and electric vehicles? | 6M | CO1 | L1 |
| | b) | Explain historical de of automobile and development of interest and activity in the EV from 1890 to present day. | 6M | CO1 | L2 |
| | | **OR** | | | |
| 3. | a) | Explain electric vehicle & its components. | 6M | CO1 | L1 |
| | b) | Explain the components of HEV and its types. | 6M | CO1 | L2 |
| | | **UNIT-II** | | | |
| 4. | a) | Which are the resistive forces that retard the motion of a four wheel vehicle? Show with a diagram. | 6M | CO2 | L1 |
| | b) | What is Battery Management System? Explain its function | 6M | CO2 | L2 |
| | | **OR** | | | |
| 5. | a) | Why Balancing Of cell is required in a Battery? Explain active cell balancing method. | 6M | CO2 | L2 |
| | b) | Discuss about fuel cell characteristics and types? | 6M | CO2 | L1 |
| | | **UNIT-III** | | | |
| 6. | | Explain with a neat sketch the working principle of Li-ion battery used in EV | 12M | CO3 | L2 |
| | | **OR** | | | |
| 7. | a) | Explain the working of DC-DC converter with neat diagram | 6M | CO3 | L2 |
| | b) | Explain the working of DC-AC converter with neat diagram | 6M | CO3 | L1 |
| | | **UNIT-IV** | | | |
| 8. | a) | What are different modes of Charging batteries? | 6M | CO4 | L2 |
| | b) | Draw and explain the block diagram of switched reluctance motor drive system. | 6M | CO4 | L1 |
| | | **OR** | | | |
| 9. | | Explain with a neat block diagram the torque control of BLDC motor | 12M | CO4 | L1 |
| | | **UNIT-V** | | | |
| 10. | a) | Explain the difference between ultra-capacitor and battery as an energy storage device for EV. | 6M | CO5 | L2 |
| | b) | What are the different battery parameters? Explain each briefly. | 6M | CO5 | L1 |
| | | **OR** | | | |
| 11. | a) | Explain rolling resistance and aerodynamic drag in vehicles. | 6M | CO5 | L2 |
| | b) | Draw a general lay out of a EV and discuss the transmission characteristics. | 6M | CO5 | L1 |

*** End ***

| Hall Ticket Number : | | | | | | | | | | |
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**R-20**

**Code: 20A453T**

III B.Tech. I Semester Supplementary Examinations June 2024

# Microprocessors and Interfacing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. In Part-A, each question carries **Two marks.**
3. Answer **ALL** the questions in **Part-A** and **Part-B**

## PART-A

**( Compulsory question )**

| | | CO | BL |
|---|---|---|---|
| 1. Answer ***all*** the following short answer questions | ( 5 X 2 = 10M ) | | |
| a) Explain the functions of sign flag. | | 1 | 2 |
| b) Differentiate near jump and far jump in 8086? | | 2 | 4 |
| c) List the modes of operation in 8255. | | 3 | 1 |
| d) What is fully nested priority mode in 8059A? | | 4 | 1 |
| e) Draw the pin diagram of USART (8251)? | | 5 | 1 |

## PART-B

**Answer *five* questions by choosing one question from each unit ( 5 x 12 = 60 Marks )**

| | | Marks | CO | BL |
|---|---|---|---|---|
| | **UNIT-I** | | | |
| 2. | Draw the architecture of 8086 microprocessor and explain the function of each unit in detail. | 12M | 1 | L2 |
| | **OR** | | | |
| 3. | What is addressing mode? Explain the following addressing modes of 8086 with suitable examples: (i) Register addressing, (ii) Based indexed addressing, (iii) Indirect addressing. | 12M | 1 | L2 |
| | **UNIT-II** | | | |
| 4. | Draw internal architecture of 8257 DMA controller and explain its programming features. | 12M | 2 | 2 |
| | **OR** | | | |
| 5. | Interface 16KX8 RAM and 16KX8 ROM to 8086. Give suitable scheme for address mapping. | 12M | 2 | 6 |
| | **UNIT-III** | | | |
| 6. a) | Explain Control word register of 8255. Write CWR for Port A as input, Port B as output and PC upper as input port, PC lower as output port. | 6M | 3 | 4 |
| b) | With the help of block diagram, explain the PPI chip. | 6M | 3 | 2 |
| | **OR** | | | |
| 7. a) | Explain the different operational modes of 8255? | 6M | 3 | 2 |
| b) | Explain how Stepper Motor controller can be connected to Microprocessor? | 6M | 3 | 6 |

## UNIT-IV

| | | | | | |
|---|---|---|---|---|---|
| 8. | | Explain the modes of operation of 8253 PIT with necessary diagram | 12M | 4 | L2 |

**OR**

| | | | | | |
|---|---|---|---|---|---|
| 9. | a) | Discuss in brief about the architecture of 8259 PIC | 6M | 1 | L1 |
| | b) | Distinguish between programmed I/O and Interrupt driven I/O. | 6M | 4 | L4 |

## UNIT-V

| | | | | | |
|---|---|---|---|---|---|
| 10. | | With the help of diagrams, explain the 8251 USART architecture and interfacing | 12M | 1 | L2 |

**OR**

| | | | | | |
|---|---|---|---|---|---|
| 11. | a) | With the help of neat diagram explain the bus structure of IEEE 488 | 6M | 5 | 2 |
| | b) | Why are the two ground pins on an RS-232C connector not just jumper together? Explain? | 6M | 5 | 4 |

*** End ***