Hall Ticket Number :										

Code: 4G365

R-14

III B.Tech. II Semester Supplementary Examinations December 2017

Digital Signal Processing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) If a system is represented by the following difference equation

$y(n) = 3y(n-1) - nx(n) + 4x(n-1) – 2\,x(n+1)$ for $n \geq 0$

Check the system for linearity, shift invariant and causality. 7M

b) Determine the unit step response of the system described by the difference equation.

$y(n) = 0.7y(n-1) – 0.1y(n-2) + 2\,x(n) – x(n-2)$ 7M

OR

2. a) Determine the response y(n), $n \geq 0$, of the system described by the second-order difference equation $y(n)-3y(n-1)-4y(n-2) = x(n)+2x(n-1)$ to the input $x(n) = 4^n u(n)$. 8M

b) State and prove Time shifting and Time reversal properties of DFT. 6M

UNIT–II

3. a) What is the computational efficiency of FFT Radix – 2 DIT algorithm for an N-point sequence? Compare it with that of direct DFT computation? 7M

b) Given a sequence x(n) = n for $0 \leq n \leq 7$, find its frequency spectrum via FFT. How do you improve the spectral resolution? 7M

OR

4. a) Explain the inverse FFT algorithm to compute inverse DFT for N=8. Draw the flow graph for the same. 7M

b) Determine the response of LTI system when the input sequence, x(n) = {-2, -1, -1, 0, 2} by radix-2 DITFFT. The impulse response of the system is, h(n) = {1, -1, -1, 1}. 7M

UNIT–III

5. a) Design a Butterworth lowpass filter for the following Specifications:

$0.8 \leq |H(e^{j\omega})| \leq 1 \qquad 0 \leq \omega \leq 0.2\pi$

$|H(e^{j\omega})| \leq 0.2 \qquad 0.6 \leq \omega \leq \pi$ 8M

b) Discuss Bilinear transformation method of deriving IIR digital filter from corresponding analog filter. 6M

OR

6. a) Design a FIR filter approximating the ideal frequency response

$H_d(e^{j\omega}) = e^{-j\alpha\omega}$, for $|\omega| \leq \pi / 6$

0, for $\pi / 6 \leq |\omega| \leq \pi$

Determine the filter coefficients for N=9. 8M

b) What is the principle of designing FIR filters using windows? 6M

UNIT–IV

7. a) Explain about the need for Multirate Digital Signal Processing? 7M

b) Consider a ramp sequence and sketch its interpolated and decimated versions with a factor ‘3’. 7M

OR

8. a) Consider the signal $x(n) = a^n u(n)$, $|a| < 1$.

(i) Determine the spectrum X(w).

(ii) The signal x(n) is applied to a decimator that reduces the rate by a factor of 2. Determine the output spectrum. 7M

b) Explain about Sampling Rate conversion of Bandpass signals. 7M

UNIT–V

9. Explain in detail about Musical Sound processing algorithm. 14M

OR

10. Write short notes on

(a) Stationary Vs. nonstationary signals 7M

(b) Oversampling A/D Converter Vs. Oversampling D/A Converter 7M

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Hall Ticket Number :										

Code: 4G363

R-14

III B.Tech. II Semester Supplementary Examinations December 2017

Microprocessors and Interfacing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Draw the block diagram of 8086 microprocessor and explain briefly. 7M

   b) Illustrate the following instructions with suitable examples:
   i) XLAT ii) MUL iii) CWD iv) DAA v) SCASB vi) SHL vii) IN 7M

OR

2. a) What do you mean by addressing modes? What are the different addressing modes supported by 8086? Explain each of them with suitable examples. 7M

   b) Write an 8086 assembly language program to and find whether a given byte is in the string or not. If it is in the string, find out the relative address of the byte from the starting location of the string. 7M

UNIT-II

3. a) Explain the control word format of 8255A in BSR mode. 7M

   b) Construct a circuit to interface ADC 0808 with 8086 using 8255 ports. Use port A for transferring digital data output of ADC to the CPU and port C for control signals. Assume that analog input is present at I/P_2 of the ADC and a clock input of suitable frequency is available for ADC. Draw the schematic and write required ALP. 7M

OR

4. a) Compare I/O mapped I/O and memory mapped I/O. 7M

   b) Create an interface between 8086 CPU and two chips of 16K *8 EPROM and two chips of 32K*8 RAM. Select the starting address of EPROM suitably. The RAM address must start at 00000H. 7M

UNIT-III

5. a) List the interrupts supported by 8086 CPU? What happens when an instruction HLT is executed? 7M

   b) What are the different operating modes of 8259? Explain each mode in detail. 7M

OR

6. a) Draw the block diagram of 8253 and explain each unit**.** 7M

   b) Develop a programmable timer using 8253 and 8086. Interface 8253 at an address 0040H for counter 0 and write ALP to interrupt the processor after 10 ms. The 8086 and 8253 run at 6 MHZ and 1.5 MHZ respectively. 7M

UNIT-IV

7. a) Distinguish between synchronous and asynchronous data transfer schemes. 7M

   b) Name the serial communication standards and draw the TTL to RS 232C and RS232C to TTL conversion circuits. 7M

OR

8. a) Give the Command instruction format in asynchronous mode of 8251A. 4M

   b) Generate a hardware interface circuit for interfacing 8251A with 8086.Set the 8251A in asynchronous mode as a transmitter with even parity enabled , 2 stop bits, 8 bit character length , frequency 160 KHZ and baud rate 10K.Write an ALP to receive 100 bytes of data string and store at 3000:4000H. 10M

UNIT-V

9. Explain the segmentation process of 80386 microprocessor 14M

OR

10. List the salient features of Pentium and Pentium pro processors . 14M

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Hall Ticket Number :										

Code: 4G362

R-14

III B.Tech. II Semester Supplementary Examinations December 2017

Microwave Engineering

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Explain the wave impedance of a rectangular waveguide and derive the expression for the wave impedance of TE and TM modes. 7M

   b) Calculate the cut-off frequency of the following modes in a square waveguide 4 cm X 4 cm TE_{10}, TM_{11} and TE_{22} 7M

OR

2. a) Derive the field expressions for a rectangular cavity resonator. Plot the field patterns for the dominant mode of propagation in such a resonator for TE and TM modes. 8M

   b) The dimensions of a guide are 2.5 X 1 cms. The frequency is 8.6 GHz. Find the following
      i. Possible modes
      ii. Cutoff frequencies
      iii. Guide wavelength 6M

UNIT–II

3. a) Write a note on waveguide irises, Posts and dielectric phase shifters. 7M

   b) Explain how a waveguide can be used as an attenuator and obtain an expression for the attenuation constant. What should be the cut off frequency and cut off wavelength of such an attenuator, for a signal propagating at 15 GHz, if the attenuation is of the order of 208 Nep/m. 7M

OR

4. a) What is a phase shifter? Explain its principle of operation linear phase changer with a neat sketch. Give its applications. 7M

   b) Describe the principle of working of a waveguide type rotary vane attenuator with neat schematics. 7M

UNIT–III

5. a) Explain E-H plane Tee junction. Why a hybrid E-H plane Tee referred to as Magic Tee. Derive the scattering matrix for E-H Tee. 8M

   b) Determine the [S] matrix of a 3-port circulator given insertion loss of 0.5 dB, Isolation of 20 dB and VSWR of 3. 6M

OR

6. a) Write the action of isolator, gyrator and circulator using ferrites. 7M

   b) Draw a neat sketch of magic T-junction. Imagine that a source is connected to arm ‘P’ and arm ‘S’ is matched terminated with reflection coefficients of 0.2 and 0.3 respectively. What is the VSWR seen by the source. 7M

UNIT–IV

7. a) Explain why there are four propagation constants in TWT and derive equations to these propagation constants. 7M

   b) Explain the π mode operation of magnetron. How to separate it from other modes. 7M

OR

8. a) Derive the expressions for output power and efficiency of a two-cavity klystron. 7M

   b) A reflex klystron operates at the peak of n=1 or ¾ mode. The D.C. power input is 40mW and ratio of V_1 to V_o is 0.278.

      i. Determine the efficiency of the reflex klystron oscillator
      ii. Find the total power output in mW.
      iii. If 20% of the power delivered by the electron beam is dissipated in the cavity walls, find power delivered to the load. 7M

UNIT–V

9. a) Give the classification of solid state μW devices along with examples. 7M

   b) Explain the GUNN effect based on two valley model theory. 7M

OR

10. a) Describe the principle of operation of IMPATT diode. 7M

    b) A KU-band IMPATT diode has a pulse operating voltage of 100V and a pulse operating current of 0.9A. the efficiency is about 10% calculate

       i. Output power
       ii. The duty cycle if the pulse width is 0.01ns and frequency is 16 GHz 7M

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Hall Ticket Number :										

R-14

Code: 4G361

III B.Tech. II Semester Supplementary Examinations December 2017

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Explain nMOS fabrication process in detail with neat diagrams? 8M
   b) Explain the process to add impurities during the fabrication process? 6M

OR

2. a) Derive an equation for I_{ds} of an n channel enhancement MOSFET operating in saturation region. 7M
   b) An n MOS transistor is operating in saturation region with the following parameters. V_{gs}=5V, V_{tn}=1.2V, (W/L) =10: $\mu_n C_{ox}$=110 $\mu A/V^2$. Find transconductance of the device. 7M

UNIT–II

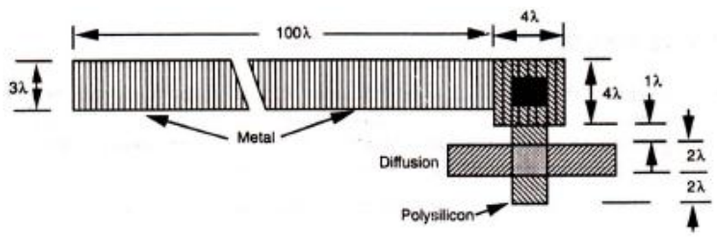
3. a) What are the alternative forms of pull ups in nMOS inverter? Write the advantages and disadvantages of each one. 8M
   b) What scaling? Explain the limitations of scaling? 6M

OR

4. a) Draw the circuit and stick diagram for AOI gate? 7M
   b) Draw the Layout for AOI gate? 7M

UNIT–III

5. a) Calculate R_{on} for nmos inverter with following parameters Z_{pu}=4 for pull up transistor and Z_{pd}=1 for pull down transistor. 6M
   b) Calculate the total capacitance associated with the structure occupying more than one layer as shown below. Use 5µm technology node?



8M

OR

6. a) Explain about nmos inverter pair delay and minimum size cmos inverter pair delay in detail. 7M
   b) Calculate the area capacitances for L=20λ,W=3λ in metal 1,polysilicon,and n type diffusion (relative capacitance for metal 1 is 0.075,polysilicon is 0.1 and n type diffusion is 0.25.) 7M

UNIT–IV

7. a) Draw and explain the FPGA architecture? 8M
   b) What is standard cell? Give its examples? 6M

OR

8. a) What is transmission gate? 4M
   b) Design an adder using transmission gate and explain with functional table? 10M

UNIT–V

9. a) What is simulation? Explain different levels of simulation? 7M
   b) What are the design strategies for test the circuit? 7M

OR

10. Explain about system level test techniques? 14M

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Hall Ticket Number :										

Code: 4G364

R-14

III B.Tech. II Semester Supplementary Examinations December 2017

Digital Communications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Draw the block diagram of PCM system and describe the function of each block in detail 7M

   b) Determine the output SNR in a DM system for a 1 kHz sinusoid sampled at 32 kHz without slope-overload and followed by 4 kHz post reconstruction filter. Also mention the advantages of digital communications systems. 7M

OR

2. a) What are the advantages of Adaptive Delta Modulation? Describe it's working principle in detail. 7M

   b) The output SNR of a 10-bit PCM was found to be 30 dB. The desired SNR is 42 dB. It was decided to increase the SNR to be the desired value by increasing the number of quantization levels *L*. Find the fractional increase in the transmission bandwidth required for this increase in *L*. 7M

UNIT–II

3. a) Derive an equation for probability of error for non-coherent PSK receiver and prove that it requires more power than coherent PSK receiver to operate at the same probability of error. 10M

   b) The carrier amplitude at the receiver input is 1 mV and power spectral density AWGN at the input is 10^{-11} W/Hz. If R_b = 5000 bps and an ideal correlation receiver is used. Calculate the bit error rate of the receiver. 4M

OR

4. a) Derive an equation for probability of error for a non-coherent quadrature PSK receiver and prove that it conserves bandwidth at the expense of power compared to binary-PSK. 7M

   b) Binary data is to be transmitted over a microwave link at a rate of 3 x 10^6 bps. Assuming the channel noise to be white gaussian with PSD of 10^{-14} W/Hz. Find the power and bandwidth requirements of four-phase PSK and 16-tone FSK signaling schemes to maintain an error probability of 10^{-4}. 7M

UNIT–III

5. a) Derive an expression for probability of error of an optimum filter. 8M

   b) Describe the working principle of operation of a baseband signal receiver. 6M

OR

6. a) State and prove the properties of a matched filter receiver. 8M

   b) Describe the principle of operation of a correlator. 6M

UNIT–IV

7. a) What is source coding theorem? Define entropy and plot entropy function of discrete memoryless source $H(p_0)$ versus 'p_0', a prior probability. 7M

   b) Apply the Shannon-Fano coding procedure for the following message ensembles $X = \{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$; P = {0.4, 0.2, 0.12, 0.08, 0,08, 0,08, 0.04}; M = 2. Find the entropy and coding efficiency? 7M

OR

8. a) What is mutual information? State and prove its properties. 7M

   b) Find the mutual information and channel capacity of the channel with channel matrix D with $P_{11} = 0.8$; $P_{12} = 0.2$; $P_{21} = 0.3$; $P_{21} = 0.7$; and $p(x_1) = 0.8$; $p(x_2) = 0.8$; 7M

UNIT–V

9. a) The generated polynomial of (7,4) cyclic code is $G(x) = 1+x+x^3$; Find the 16 code words of this systematic cyclic code. 7M

   b) Design an encoder for the (7, 4) systematic cyclic code generated by $G(x) = 1+x+x^3$; also verify its operation for any one message word. 7M

OR

10. For a (3, 1, 2) convolution encoder if g1 = [1 1 0]; g2 = [1 0 1], then draw (i) tree diagram; (ii) state diagram; and (iii) Trellis diagram 14M

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