| Hall Ticket Number : | | | | | | | | | | |
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**Code: 4G364**

**R-14**

*III B.Tech. II Semester Regular Examinations May 2017*

# Digital Communications

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit ( 5 x 14 = 70 Marks )

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## UNIT–I

1. a) Derive an equation for SNR of a PCM system and prove that each bit in the code word of a PCM contributes 6 dB to the SNR. 7M

   b) In a binary PCM system, the signal to quantization noise ratio is to be held to a minimum of 40 dB. Determine the number of quantization levels required and find the corresponding signal to quantization noise ratio. Also describe the problems (disadvantages) of Delta modulation. 7M

**OR**

2. a) Draw the block diagram of a digital communication system and describe the function of each block. Also mention the advantages of digital communication systems. 10M

   b) A delta modulation system is designed to operate at five times the Nyquist rate for a signal with 3 kHz bandwidth. Determine the maximum amplitude of 2 kHz input sinusoid for which the delta modulator does not have slope-overload and with quantization step size of 250 mV. 4M

## UNIT–II

3. a) Derive an equation for probability of error of a coherent FSK receiver. 7M

   b) Binary data is transmitted over a telephone line with usable bandwidth of 2400 Hz using FSK signaling scheme. The transmit frequencies are 2025 and 2225 Hz and data rate is 300 bps. The average SNR at the output of the channel is 6 dB. Calculate the probability of error for coherent and non- coherent schemes. 7M

**OR**

4. a) Derive an equation for probability error of a coherent ASK receiver. 7M

   b) Binary data is to be transmitted over a microwave link at a rate of $3 \times 10^6$ bps. Assuming the channel noise to be white gaussian with PSD of $10^{-14}$ W/Hz. Find the power and bandwidth requirements of four-phase PSK and 16-tone FSK signaling schemes to maintain an error probability of $10^{-4}$. 7M

## UNIT–III

5. a) State and prove the properties of a matched filter receiver. 8M

   b) Describe the principle of operation of a correlator. 6M

**OR**

6. a) Derive an expression for probability of error of an optimum filter. 8M

   b) Describe the working principle of operation of a baseband signal receiver. 6M

## UNIT–IV

7. a) What is entropy? State and prove its properties. 8M

   b) A discrete memoryless source with source alphabet S = {$s_0$, $s_1$, $s_2$} with respective probabilities {¼, ¼, ½}. Find the entropy of the source? Also find the entropy of this second order extension discrete memory less source. What do you observe from the two results? Give the conclusion. 6M

**OR**

8. Consider a sequence of letters of the English alphabet of seven symbols whose probabilities of occurrences: Letters: {*a, i, l, m, n, o, p, y*}; Probability: {0.1, 0.1, 0.2, 0.1, 0.1, 0.2, 0.1, 0.1}. Compute two different Huffman for this alphabet. In one case move a combined symbol in the coding procedure as high as possible, and in the second case, move it as low as possible. Hence, for each of the codes, find the average code-word length and variance of average code-word length over the ensemble of letters. 14M

## UNIT–V

9. a) Design a block code with a minimum distance of 3 and a message block size of 8 bits. 7M

   b) The generated polynomial of (7, 4) cyclic code is $G(x) = 1+x+x^3$; Find the 16 code words of this code. 7M

**OR**

10. For a (3, 1, 2) convolution encoder if g1 = [1 1 0]; g2 = [1 0 1], then draw
    (i) tree diagram; (ii) state diagram; and (iii) Trellis diagram 14M

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| Hall Ticket Number : | | | | | | | | | | |
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**R-14**

**Code: 4G365**

*III B.Tech. II Semester Regular Examinations May 2017*

# Digital Signal Processing

( Electronics and Communication Engineering )

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit ( 5 x 14 = 70 Marks )

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## UNIT–I

1. a) Check the following systems for linearity, causality, time invariance and stability using appropriate tests
   i) $y(n) = ne^{|x(n)|}$
   ii) $y(n) = a^n \cos(2\pi n/N)$ 8M

   b) Determine the response of a relaxed system characterized by the impulse response $h(n) = (1/2)^n u(n)$ to the input signal $x(n) = u(n)$. 6M

**OR**

2. a) Consider two periodic sequences x(n) and y(n), x(n) has period N and y(n) has period M. The sequence w(n) is defined as w(n) = x(n) + y(n).
   (i) Show that w(n) is periodic with period MN.
   (ii) Determine W(K) in terms X(K) and Y(K) where X(K), Y(K) and W(K) are the Discrete Fourier series coefficients with a period of N, M and MN respectively. 7M

   b) Define DFT of a sequence. Compute the N - point DFT of the sequence.
   $x(n) = \cos(2\pi rn/N)$, $0 \le n \le N-1$ and $0 \le r \le N-1$ 7M

## UNIT–II

3. a) Explain the symmetry conditions in DFT, which permit the development of FFT algorithms. 7M

   b) Compute the IDFT of the following sequence using FFT algorithm
   X(K) = {5,0,1-j,0,1,0,1+j,0} 7M

**OR**

4. a) Compute the DFT for the sequence {1, 0, 0, 0, 0, 0, 0, 0} using DIFFFT algorithm. 7M

   b) Give the steps involved in implementing Radix –3, DIT FFT algorithm. 7M

## UNIT–III

5. a) Design a Chebyshev IIR LPF for the following specifications:

$$0.87 \le \left|H(e^{j\mu})\right| \le 1.0, \quad 0 \le \mu \le 0.25®$$

$$\left|H(e^{j\mu})\right| \le 0.35, \quad 0.375® \le \mu \le ®$$

   7M

   b) Obtain the direct form I and direct form II realization for the following system.
   y(n) = -0.1y(n-1)+0.2y(n-2)+3x(n)+3.6x(n-1)+0.6x(n-2) 7M

**OR**

6. a) Design a Linear-phase FIR lowpass filter with the following desired frequency response using Hamming window for N=7.

$$H_d(e^{j\omega}) = \begin{cases} 1 & for\ 0 \le |\omega| \le \frac{\pi}{4} \\ 0 & for\ \frac{\pi}{4} \le |\omega| \le \pi \end{cases}$$

   8M

   b) Explain briefly the method of designing FIR filter using Frequency sampling method. 6M

**UNIT–IV**

7. a) Explain the Decimation process in time domain and frequency domain. 7M

   b) Explain the concept of multirate signal processing with spectral interpretation of decimation of a signal from 6 KHz to 2 KHz and spectral interpretation of interpolation of signal from 2 KHz to 6 KHz. 7M

**OR**

8. a) Plot the signals and their corresponding spectra for rational sampling rate conversion by (a) I / D =5 / 3 and (b) I / D =3 / 5. Assume that the spectrum of the input signal x(n) occupies the entire range $-\pi \leq w_x \leq \pi$. 7M

   b) Explain about the sampling rate conversion by a rational factor I/D. 7M

**UNIT–V**

9. Explain about various steps followed in signal compression. 14M

**OR**

10. Write short notes on

    (a) A/D converters 7M

    (b) D/A converters 7M

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| Hall Ticket Number : | | | | | | | | | | |
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**Code: 4G363**

**R-14**

*III B.Tech. II Semester Regular Examinations May 2017*

# Microprocessors and Interfacing

( Electronics and Communication Engineering )

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit ( 5 x 14 = 70 Marks )

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## UNIT–I

1. a) Describe the purpose of BIU and EU in 8086 microprocessor. 7M

   b) Illustrate the following instructions with suitable examples:
   i) LOOP ii) DIV iii) CBW iv) TEST v) MOVSB vi) SHR vii) CMPSB 7M

**OR**

2. a) Compare the architectures of 8085 and 8086 microprocessors 7M

   b) Develop a 8086 assembly language program to move a string of data words from offset 2000H to offset 3000H. The length of the string is FFH 7M

## UNIT-II

3. a) Explain the control word format of 8255A in I/O and BSR mode. 7M

   b) Construct a circuit to interface 16 bit 8255 ports with 8086. The address of port A is F0H. 7M

**OR**

4. a) Distinguish between I/O mapped I/O and memory mapped I/O. 7M

   b) Create an interface circuit of two 4K*8 EPROMS and two 4K*8 RAM chips with 8086 microprocessor. 7M

## UNIT-III

5. a) What are the key differences between NMI and other external hardware interrupts? 7M

   b) Discuss the internal architecture of 8259A with the help of block diagram 7M

**OR**

6. a) Discuss the different modes of operation of 8253**.** 7M

   b) Develop a programmable timer using 8253 and 8086.Interface 8253 at an address 0040H for counter 0 and write ALP to generate a square wave of period 1ms. The 8086 and 8253 run at 6 MHZ and 1.5 MHZ respectively. 7M

## UNIT-IV

7. a) Classify the various data transfer schemes. 7M

   b) Name the serial communication standards and draw the TTL to RS 232C and RS232C to TTL conversion circuits. 7M

**OR**

8. a) Define the mode instruction format in asynchronous mode of 8251A. 4M

   b) Generate a hardware interface circuit for interfacing 8251A with 8086.Set the 8251A in asynchronous mode as a transmitter with even parity enabled , 2 stop bits, 8 bit character length , frequency 160 KHZ and baud rate 10K.Write an ALP to transmit 100 bytes of data string starting at location 2000:5000H 10M

## UNIT-V

9. List the salient features of 80386 microprocessor. 14M

**OR**

10. Compare the Pentium and Pentium pro processors. 14M

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| Hall Ticket Number : | | | | | | | | | | |
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**Code: 4GA62**

**R-14**

*III B.Tech. II Semester Regular Examinations May 2017*

# Management Science

( Electronics and Communication Engineering )

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit ( 5 x 14 = 70 Marks )

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## UNIT–I

1. a) Define Management? Explain the characteristics of Management? 7M

   b) Explain the Importance of Management? 7M

**OR**

2. Discuss the features of line and staff organization. For what type activities it is best suited? 14M

## UNIT–II

3. Explain the steps in Plant Layout? What are the various merits and demerits of process layout? 14M

**OR**

4. Define Inventory Management? What are the techniques of Inventory Management? Discuss? 14M

## UNIT–III

5. Define the term Marketing? Mention and evaluate the prominent channels of distribution? 14M

**OR**

6. What is performance appraisal? Discuss in brief the methods of performance appraisal? 14M

## UNIT–IV

7. Define Financial Management? Briefly discuss its scope? 14M

**OR**

8. With the help of the following data, draw the network. (**a**) Draw the network (**b**) Find project duration for the following project and (**c**) Identify the critical path

| Activity | 1-2 | 1-3 | 1-4 | 2-4 | 2-5 | 3-4 | 3-7 | 4-6 | 4-7 | 5-6 | 5-7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Time (months) | 4 | 6 | 12 | 7 | 11 | 7 | 8 | 8 | 13 | 4 | 4 |

14M

## UNIT–V

9. What is Enterprise Resource Planning? Where it is applicable? Explain in detail? 14M

**OR**

10. What is Just-In-Time? Explain its features, advantages and disadvantages? 14M

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| Hall Ticket Number : | | | | | | | | | | |
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**Code: 4G362**

**R-14**

*III B.Tech. II Semester Regular Examinations May 2017*

# Microwave Engineering

( Electronics and Communication Engineering )

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit ( 5 x 14 = 70 Marks )

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## UNIT–I

1. a) Derive the TM $_{m n}$ mode field equation in rectangular waveguide 7M

   b) What are dominated and degenerate modes? What is the significance of dominant modes? Indicate the dominant mode in rectangular wave guide and calculate $f_c$ for the same. 7M

**OR**

2. a) Derive the expression for the characteristic impedance of micro strip lines 8M

   b) Find the first five resonances of an air-filled rectangular cavity with dimensions of a = 5 cms, b= 4 cms and c= 10 cms (d>a>b) 6M

## UNIT–II

3. a) Derive the expression for Rectangular cavity resonator 6M

   b) A rectangular waveguide has dimensions 2.5 X 5 cms. Determine the guide wavelength, phase constant and phase velocity at a wavelength of 4.5 cms for dominate mode. 8M

**OR**

4. a) Explain Coupling probes and coupling loops 7M

   b) What is phase shifter? Explain its principles of operation with a neat sketch. Give its applications. 7M

## UNIT–III

5. a) Derive the scattering matrix of H-plane Tee? 7M

   b) What are the properties of S matrix? Derive the scattering matrix for a 3 port circulator? 7M

**OR**

6. a) Explain Coupling factor, Directivity and Isolation using Directional coupler. 5M

   b) What is meant by Microwave Attenuator? Explain the functioning of flap and vane Attenuators. 9M

## UNIT–IV

7. a) Draw the equivalent circuit of a reflex klystron and discuss electronic admittance in detail. Use relevant expression and plots. Mention the performance characteristics of reflex klystron? 8M

   b) Two cavity klystron is operated at 10GHz with $V_o$=1200V, $I_o$ = 30mA, d=1mm, L=4cm and $R_{sh}$=40KΩ.Calculate

      i) Input RF voltage $V_1$ for a maximum output voltage,

      ii) Voltage Gain

      iii) Efficiency 6M

**OR**

8. a) Explain the principle of operation of a two-cavity klystron with a neat diagram? 7M

   b) The operating frequency of a reflex klystron is 5 GHz it has a DC beam of 250V, a repeller spacing of 0.1 cm for 1 ¾ mode. Determine the maximum value of power and the corresponding repeller voltage for a beam current of 60mA. 7M

## UNIT–V

9. a) Explain the construction of GUNN diode using RWH theory. 7M

   b) What is TRAPATT diode and explain the principle of operation? 7M

**OR**

10. a) What is meant by Avalanche Transit Time Devices? Explain the operation, construction and application of IMPATT. 7M

    b) The helical TWT has diameter of 2 mm with 50 turns per cm. Calculate axial phase velocity and a node voltage at which the TWT can be operated for useful gain. 7M

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| Hall Ticket Number : | | | | | | | | | | |
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**R-14**

**Code: 4G361**

*III B.Tech. II Semester Regular Examinations May 2017*

# VLSI Design

( Electronics and Communication Engineering )

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit ( 5 x 14 = 70 Marks )

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**UNIT–I**

1. a) Explain CMOS fabrication using N-well process with neat diagrams. 8M
   b) Explain about lithography process to pattern the oxide layer. 6M

**OR**

2. a) Determine the Pull-up to Pull-down ratio for an nMOS inverter driven by another nMOS inverter? 8M
   b) Draw the Bi-CMOS inverter with no static current flow and give its advantages. 6M

**UNIT–II**

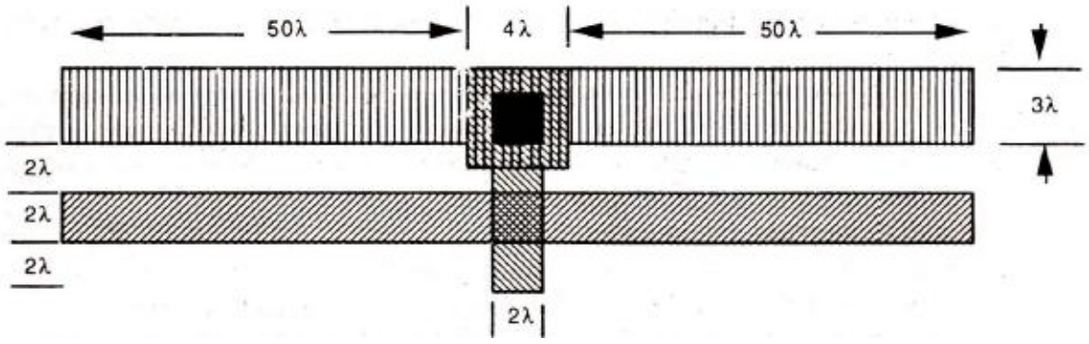
3. a) Explain the CMOS inverter in all aspects and derive the expression for $V_{in}$ and in that expression what is the role of $(\beta_n/\beta_p)$. 8M
   b) Draw the 3 input AND gate using pass transistor logic. 6M

**OR**

4. a) Draw the circuit and stick diagram for OAI gate? 7M
   b) Draw the Layout for OAI gate? 7M

**UNIT–III**

5. a) Calculate inverter resistance for nMOS with $Z_{pu}$=4 for pull up transistor and $Z_{pd}$=1for pull down transistor and for CMOS $Z_{pu}$=1 for pull up transistor and $Z_{pd}$=1 for pull down transistor. 7M
   b) Calculate the total capacitance associated with the structure occupying more than one layer as shown below. Use 5µm technology node?




7M

**OR**

6. a) Explain the importance of wiring capacitances along with classifications? 7M
   b) Explain different switch logic used for designing of VLSI circuits? 7M

**UNIT–IV**

7. a) Design an array multiplier and discuss the merits and demerits with an example? 7M
   b) Explain a zero/one detector with application? 7M

**OR**

8. a) Write the applications of CPLD? 6M
   b) What is CLB? Explain its structure? 8M

**UNIT–V**

9. a) What is testing? Discuss the importance of testing? 6M
   b) Discuss about design capture tools and design verification tools? 8M

**OR**

10. a) What are the test principles to test the circuit? 6M
    b) Explain about chip level test techniques? 8M

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