Code : 1G364

R11

III B.Tech. II Semester Supplementary Examinations December, 2014

Digital and Data Communications

(ECE)

Time: 3 hours **Max Marks: 70**

Answer any FIVE of the following
All questions carry equal marks (14 Marks each)

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1. a) Explain Digital Communication System using a neat diagram? 6M

   b) A signal $m(t)=\cos(200\pi t)+2\cos(320\pi t)$ is ideally sampled at 300 Hz. If the sampled signal is passed through a low pass filter with cut-off frequency 250 Hz. What frequency components will appear at the output? 8M

2. a) Sketch the block diagrams of QPSK modulator and coherent QPSK Demodulator. Discuss the role of each block? 10M

   b) Differentiate ASK and FSK? 4M

3. a) State and Prove Sampling theorem in Time Domain? 7M

   b) What is matched filter? Derive Expression for its output SNR? 7M

4. a) Explain Huffman encoding Algorithm? 8M

   b) A discrete memory less source has an alphabet of five symbols whose probabilities of occurrence as described below:

Symbols:-	s_0	s_1	s_2	s_3	s_4
Probabilities:-	0.4	0.2	0.2	0.1	0.1

   Compute the Huffman code for this source, entropy and average code word length of the source encoder. 6M

5. a) The Generated matrix for a (6,3) block code is given below:

   $$G = \begin{pmatrix} 1\,0\,0 & 1\,1\,0 \\ 0\,1\,0 & 0\,1\,1 \\ 0\,0\,1 & 1\,1\,1 \end{pmatrix}$$

   Find all code vectors for this code? Consider any one message block contains an error to correct that by using syndrome calculations. 10M

   b) Explain sequential decoding of convolution code? 4

6. a) Briefly explain Layered Network Architecture? 7M

   b) List and describe the standard organizations for data communications? 7M

7. a) Explain the characteristics of Logical Link Control (LLC)? 6M

   b) Describe in detail about Error-detection mechanisms? 8M

8. a) Explain different traffic control functions defined for maintaining ATM connections? 6M

   b) How do you provide Network security in application layer? 8M

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Code : 1G363

R11

III B.Tech. II Semester Supplementary Examinations December, 2014

Microprocessors and Interfacing

(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 70**

Answer any FIVE of the following

All questions carry equal marks (14 Marks each)

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1.	a)	Describe architecture of 8086 with neat diagram.	7M
	b)	Write note on memory organization in 8086 processor.	7M
2.	a)	Write note on different addressing modes available in 8086 processor with one example each.	10M
	b)	Write assembly language program to sort 10 numbers in ascending order using bubble sort technique.	4M
3.	a)	What is 8255? Explain how 8255 can be used to extend the ports available in microprocessor? What are different modes available in 8255?	9M
	b)	Explain how a uni-polar stepper motor can be interfaced. Write assembly language program to rotate stepper motor 90 degrees clock wise first and then 36 degrees antilock wise. Assume step angle of stepper motor is 1.8 degrees	5M
4.	a)	Write note on basic structures of SRAM and DRAM cells with neat diagram.	5M
	b)	What is meant by DMA? Explain the architecture of 8257.	9M
5.	a)	Explain about DOS and BIOS interrupts.	7M
	b)	Write note on different data transfer methods.	7M
6.	a)	Explain the internal architecture of 8253. What are different operating modes of 8253?	7M
	b)	Explain how 8279 is interfaced with 8086 microprocessor.	7M
7.	a)	Explain asynchronous and synchronous serial data transfer schemes.	7M
	b)	Write a simple assembly program for serial data transfer.	7M
8.	a)	Write note on salient features of Pentium and Pentium pro processors	7M
	b)	Explain the concept of paging in detail	7M

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Code : 1GA62

R11

III B.Tech. II Semester Supplementary Examinations December, 2014

Management Science

(*Electronics & Communication Engineering*)

Time: 3 hours **Max Marks: 70**

Answer any FIVE of the following

All questions carry equal marks (14 Marks each)

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1. The logical sequence of management functions cannot be subordinated even by one function. Do you agree? Support your answer

2. The following data represents the No of defects found on each sewing machine cabinet inspects. Plot a Control chart with control limits. Comment on the chart

Sample number	1	2	3	4	5	6	7	8	9	10
No of Defects	8	10	7	9	6	7	8	9	4	5

3. Define Marketing. How is it different from selling? Explain how marketing starts and ends with the customer

4. Explain the important stages in the manpower planning function

5. Is there any link between Mission, Goal, Objective, Strategy and Programmes in an Industrial environment? Illustrate.

6. Explain the nature of costs in a project. Discuss how the project manager should go about analyzing the costs which different activities are to be crashed in a project.

7. Discuss the significance of TQM

8. Explain the ethical issues in various functional areas of Management

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Code : 1G362

R11

III B.Tech. II Semester Supplementary Examinations December, 2014

Microwave Engineering

(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 70**

Answer any FIVE of the following
All questions carry equal marks (14 Marks each)

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1. a) How are waveguides different from normal two wire transmission lines? Discuss in detail about their similarities and dissimilarities.
   b) A Rectangular waveguide of cross section 5cm x 2cm is used to propagate TM11 at 9 GHZ. Determine
      i) Cut off wavelength
      ii) Cut off frequency
      iii) Wave impedance
2. a) Determine the Expressions for field components for TE Waves in Circular Waveguide?
   b) Define Quality Factor and derive quality factor for TE_{01} mode of Rectangular cavity resonator?
3. a) Discuss the need to use Scattering Matrix at the Microwave Frequencies and mention its properties. Also derive the scattering matrix relation between the input and output of a nxn junction.
   b) What E-H plane Tee? Explain the relation among the ports with S matrix and also justify why it is so called magic Tee.
4. a) Explain the construction, working and applications of a 3 port Circulator.
   b) Determine the scattering parameters for a 10-dB direction Coupler. The Directivity D=30dB. Assume that it is lossless and the VSWR at each port is 1.0 under matched conditions.
5. Discuss about the velocity and current modulation of a two-cavity Klystron Amplifier using apple gate diagrams. Derive the expressions for its output power and efficiency
6. a) Draw the Labeled Schematic diagram of Helix TWT, and show that the output power gain of Helix TWT is G= -9.54 + 47.3NC db?
   b) What is Phase focusing effect? Explain the effect in magnetron.
7. a) Explain the characteristics of a Gunn diode based on RWH Theory
   b) Explain the how negative resistance is exhibited in IMPATT and TRAPATT.
8. a) With a neat sketch explain the Impedance measurement techniques.
   b) With a neat sketch explain the VSWR measurement techniques.

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Code : 1G361

R11

ANNAMACHARYA INSTITUTE OF TECHNOLOGY & SCIENCES :: RAJAMPET
(AUTONOMOUS)

III B.Tech. II Semester Supplementary Examinations December, 2014

VLSI Design

(*Electronics & Communication Engineering*)

Time: 3 hours **Max Marks: 70**

Answer any FIVE of the following
All questions carry equal marks (14 Marks each)

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1.	a)	What is Moore's law? Explain it relevance with respect to evolution of technology	6M
	b)	Explain CMOS fabrication using P-well process with neat sketches	8M
2.	a)	Explain latch-up problem in CMOS circuits	6M
	b)	Explain various regions of CMOS inverter transfer characteristics	8M
3.	a)	Design a stick diagram for three input NOR gate using NMOS logic	6M
	b)	Write the scaling factors for different types of device parameters	8M
4.		Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.	14M
5.	a)	Write a short note on Zero/One detectors.	8M
	b)	Design a magnitude comparator based on the data path operators.	6M
6.	a)	Write briefly about channeled gate arrays.	6M
	b)	Implement 2-bit comparator using PROM	8M
7.		With respect to synthesis process explains the following. 1. Flattening 2. Factoring 3. Mapping	14M
8.	a)	Draw the state diagram of TAP controller and explain how it provides the control signals for test data and instruction register.	8M
	b)	Explain how an improved layout can reduce faults in CMOS circuits.	6M

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