Hall Ticket Number :										

R-11 / R-13

Code: 1G468

III B.Tech. II Semester Supplementary Examinations May 2019

Computer System Architecture

(Electrical and Electronics Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) Convert the following
   i. $(756)_{10} = (?)_8$
   ii. $(175)_{16} = (?)_{10}$
   iii. $(1362)_8 = (?)_2$
   iv. $(1110101)_2 = (?)_{10}$
   v. $(F3A7C2)_{16} = (?)_8$ 10M

   b) Draw and illustrate single bus structure in computer. 4M

2. a) With neat diagram explain binary adder-subtractor and incrementer. 7M

   b) List out the registers needed by the basic computer. 7M

3. List and explain instruction formats in brief. 14M

4. a) Elaborate the process of mapping of instructions in control memory. 7M

   b) Explain microprogram sequencer in microprogrammed control unit. 7M

5. a) How addition and subtraction with signed magnitude data perform? Explain with flow chart. 7M

   b) Write a flow chart for multiplication of floating point numbers. 7M

6. a) Explain auxiliary Memory block diagram in detail. 9M

   b) Define address space and Memory Space in virtual memory. Explain with an example. 5M

7. a) List and describe the peripheral devices in computer. 7M

   b) Explain interrupt cycle with neat sketch. 7M

8. a) Compare and contract serial and parallel arbitration in interprocessor arbitration. 8M

   b) Describe delayed load in RISC pipeline. 6M

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Hall Ticket Number :										

R-11/R-13

Code : 1G366

III B.Tech. II Semester Supplementary Examinations May 2019

Microprocessors and Microcontrollers

(Electrical & Electronics Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1. Bring out the differences between MIN & MAX modes of 8086. Explain how the Bus control signals are obtained in Maximum mode. 14M

2. a) With suitable examples, bring out the similarities and differences between Procedure and Macro. 8M

   b) It is required to perform sum of two 16-bit numbers. Implement it with four different addressing modes. 6M

3. a) Compare the memory mapped I/O and the I/O mapped I/O in 8086. 7M

   b) List out the different Programmable and non Programmable interfacing devices. 7M

4. A memory system is to be designed for an 8086 processor based system with two chips of 16K X 8 EPROM and two chips of 32K X 8 RAM. Select the suitable memory map based on 8086 microprocessor's architecture. 14M

5. Draw and explain the internal structure of (8259) Programmable interrupt controller. 14M

6. a) Write the features of RS-232C serial communication standard. 7M

   b) Explain the features of Universal serial bus. 7M

7. a) Contrast interrupts and polling. Explain the interrupt handling mechanism in 8051 microcontroller. 7M

   b) What are the interrupts in 8051 microcontroller? Explain their priorities, call addresses and priority handling. 7M

8. a) Discuss the memory organization of MCS-96 microcontroller. 7M

   b) Compare 8051 and ARM microcontrollers. 7M

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Hall Ticket Number :										

R-11 / R-13

Code: 1G263

III B.Tech. II Semester Supplementary Examinations May 2019

Power System Operation and Control

(Electrical and Electronics Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) Explain the following terms concerned to a thermal power plants and their significance.
   (i) Incremental input (ii) Production cost
   (iii) Generation cost (iv) Heat rate – power output curve 6M

   b) In a three plant system the cost functions are given by

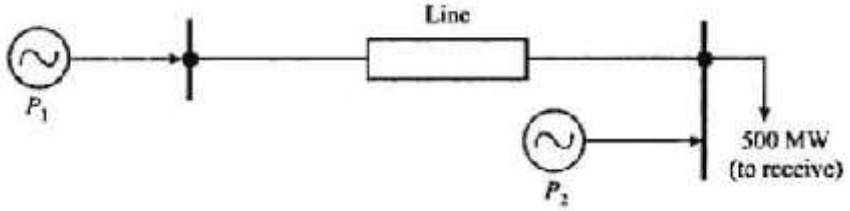
$$F_1 = 500 + 7P_1 + 0.002P_1^2 \quad Rs./hr; \quad 100 \le P_1 \le 500$$

$$F_2 = 400 + 6.5P_2 + 0.003P_2^2 \quad Rs./hr; \quad 100 \le P_2 \le 300$$

$$F_3 = 200 + 7.2P_3 + 0.006P_3^2 \quad Rs./hr; \quad 100 \le P_3 \le 300$$

   Where P_1, P_2 and P_3 are the real power generation of each unit. Determine the economical load allocation between the three units, when the total load on the station is 900 MW. 8M

2. The losses in the lines shown in the figure are proportional to the square of the power flow. Both units are loaded to 250 MW. Due to transmission losses 12.5 MW power is lost. Where should be the extra 12.5 MW be generated for economic operation? Attempt the rescheduling to minimize the transmission losses. The maximum and minimum generation constraints on the plants are 400 MW and 70 MW.



14M

3. a) Derive the co-ordination equations for the optimal scheduling of hydro-thermal interconnected power plants. 6M

   b) In a two plant operation system, the hydro plant is operation for 10 hrs, during each day and the steam plant is to operate all over the day. The characteristics of the steam and hydro plants are:

$C_T = 0.04\ P_{GT}^{\ 2} + 30\ P_{GT} + 10$ Rs/hr.

$W_H = 0.12\ P_{GH}^{\ 2} + 30\ P_{GH}$ m^3/ sec.

   When both plants are running, the power flow from steam plant to load is 150 MW and the total quantity of water is used for the hydro plant operation during 10 hrs is 150×106 m^3. Determine the generation of hydro plant and cost of water used. Neglect the transmission losses. 8M

4. a) From the fundamentals develop the functional block diagram representation of a speed governor system. 6M

   b) Two generators rated 100MW and 200MW are operating in parallel. The droop characteristics of their governors are 3% and 5% respectively from no load to full load. Assuming that the generators are operating at 50 Hz at no load, how would a load of 300 MW be shared between them? What will be the system frequency at this load? Assume free governor operation. 8M

5. a) Show that the steady state error of frequency in a typical LFC of a power system is reduced to zero using an appropriate controller. 6M

   b) A single area system has the following data: Speed Regulation, R=5 Hz/pu.MW, Damping coefficient, B=0.2pu MW/Hz Power system time constant, Tp=12 sec, Power system gain, Kp=80 hz/pu.MW When a 3% load change occurs, determine Area Frequency Response characteristic (AFRC) and the static frequency error. What is the value of steady state frequency error if the governor is blocked? 8M

6. a) Define the concept of control area and its functional responsibilities in an interconnected power system. 6M

   b) Two areas are connected via an inter tie line. The load at 50 Hz, is 15000 MW in area 1 and 35000 in area 2. Area 1 is importing 1500 MW from area 2. The load damping constant in each area is B=1.0 and the regulation R=6 % for all units. Area 1 has a spinning reserve of 800 MW spread over 4000 MW of generation capacity and area 2 has a spinning reserve of 1000 MW spread over 10000 MW generation. Determine the steady state frequency, generation and load of each area and tie-line power for
      i. Loss of 1000 MW in area2, with no supplementary control.
      ii. Loss of 1000 MW in area2, with supplementary controls provided on generators with reserve. 8M

7. a) Explain clearly what do mean by compensation of a line and discuss briefly different methods of compensation. 6M

   b) A 220 kV line has tap changing transformer at both the ends. The transformer at the sending end has a nominal ratio of 11 220 kV and that at the receiving end is 220/11 kV. The line impedance is (20 + j 60) ohms and the load at the receiving end is 100 MVA, 0.8 p.f. lagging. If the product of two off nominal tap settings is 1, find the tap settings to give 11 kV at load bus. 8M

8. a) What are the key issues in deregulated Power Systems? 6M

   b) Explain the structure of deregulated electric industry. How does it differ from vertically integrated electric industry? 8M

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