Hall Ticket Number :										

R-11 / R-13

Code: 1G364

III B.Tech. II Semester Supplementary Examinations May 2017

Digital and Data Communications

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **Five** questions
All Questions carry equal marks (**14 Marks** each)

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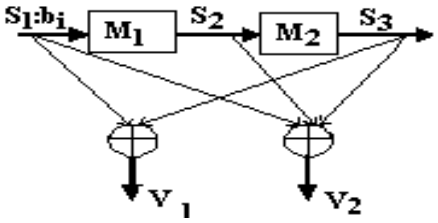
1. a) Explain with a neat block diagram the operation of a continuously variable slope delta modulator (CVSD). 7M
   b) Compare Delta modulation with Pulse code modulation technique. 7M
2. a) Explain with neat diagrams coherent BFSK transmitter and receiver. Explain single space diagram for coherent BFSK systems. 7M
   b) With a neat diagram explain QPSK receiver scheme. Give also the phasor diagram of QPSK. 7M
3. a) Explain what is meant by coherent detection and draw a block diagram of a coherent BPSK receiver. 7M
   b) Find the bit error probability for a BPSK system with a bit rate of 1 Mbit/s. The received waveforms, $s_1(t) = A\cos w_0 t$ and $s_2(t) = -A\cos w_0 t$, are coherently detected. The value of A is 10 mV. Assume that the single–sided noise power spectral density is $N_0 = 10^{-11} W/Hz$ that signal power and energy per bit are normalized relative to a 1 Ω load. 7M
4. a) Briefly Explain Shannon-Fano algorithm with an example. 7M
   b) Calculate the bandwidth limits of Shannon-Hartley theorem. 7M
5. a) Explain the encoding Principle in Convolutional Code. 6M
   b) Find the Output of the following Convolutional Encoder for an input data of 10011



8M

6. a) Write short notes on the following:
      i) Protocols and Standards.
      ii) State the responsibilities of Network layer. 7M
   b) How do you the layers of the Internet model correlate to the layers of the OSI model. 7M
7. a) List and describe the standards Flags of a UART Standard register. 7M
   b) List and describe the two types of loopbacks associated with DTE and DCEs. 7M
8. a) Describe the fields that comprises an X.25 call request packet. 5M
   b) Describe how access to BISDN network is achieved. 5M
   c) List the ATM network components. 4M

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Code: 1G365

III B.Tech. II Semester Supplementary Examinations May 2017

Electronic Measurements and Instrumentation

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **Five** questions
All Questions carry equal marks (**14 Marks** each)
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1.	a)	Explain how the Range of D.C voltmeter is extended?	7M
	b)	What are errors Define following errors with examples. i) Instrumental Errors ii) Limiting errors	7M
2.	a)	Sketch the block diagram of QSPK modulator and coherent QSPK demodulator.	7M
	b)	Design a universal aryton shunt to provide an ammeter with a current range of 2A, 5A, and 10A using a D' arsonval movement with an internal resistence R_m =50 ohms and full scale deflection current of 1mA.	7M
3.	a)	State and prove Sampling theorem in Time domain.	7M
	b)	Explain the front –panel description of Signal generator?	7M
4.		Draw the neat diagrams of vertical and horizontal deflection systems of CRO and explain their working in detail	14M
5.		Explain the operation of Storage Oscilloscope with a neat block diagram?	14M
6.	a)	Explain the working of wheat stone bridge and derive the equation for balance condition and unbalance condition.	7M
	b)	Find the equivalent parallel resistence and capacitance that causes a Wien bridge to null with the following component values. R_1=2k ohms, C_1=0.1μF, R_2=10K ohms, R_3=50K ohms, R_4=20K ohms , ω =1KHz.	7M
7.	a)	Explain the characteristics of Logical Link Control (LLC)	7M
	b)	Explain the Piezo – electric effect in detail?	7M
8.	a)	Draw the block diagram of Strip – chart recorder and explain its working.	7M
	b)	How do you provide Network security in application layer?	7M

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R-11 / R-13

Code: 1G363

III B.Tech. II Semester Supplementary Examinations May 2017

Microprocessors and Interfacing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **Five** questions
All Questions carry equal marks (**14 Marks** each)

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1. a) With a neat block diagram explain the architecture of 8086 processor. 7M
   b) Explain why memory is segmented in 8086 and also explain how memory is addressed using segmentation. 7M

2. a) What is MACRO? Explain nested macro with examples. 6M
   b) Develop an 8086 assembly language program to sort a given set of 16-bit unsigned integers into ascending order using insertion sort technique. 8M

3. a) Explain how Stepper Motor controller can be connected to Microprocessor. 7M
   b) Explain the different modes of 8255. 7M

4. a) Draw internal architecture of 8257 DMA controller, and explain its programming features. 6M
   b) Explain the following:
      i. Mask programmed ROM.
      ii. Erasable programmable ROM (EROM).
      iii. Programmable ROMs (PROMs).
      iv. Electrically programmable ROM (EEROMs). 8M

5. a) Explain Interrupt structure of 8086 and Vector interrupt table. 7M
   b) Briefly explain about DOS and BIOS interrupts 7M

6. a) Explain various operating mode of 8253 timer. 6M
   b) Describe the working of a 4 × 4 hexadecimal matrix keyboard interfaced through the ports of 8255. Give the hardware and software for it. 8M

7. a) A terminal is transmitting asynchronous serial data at 1200 Bd. What is the bit time? Assuming 8 data bits, a parity bit and 1 stop bit, How long does it take to transmit one character? 8M
   b) Why are the two ground pins on an RS-232C connector not just jumpered together? 6M

8. a) Enlist the salient features of 80286, 80386, and 80486. 8M
   b) Explain the architecture of Pentium Processor. 6M

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Hall Ticket Number :										

R-11 / R-13

Code: 1G362

III B.Tech. II Semester Supplementary Examinations May 2017

Microwave Engineering

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **Five** questions
All Questions carry equal marks (**14 Marks** each)

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1. a) Drive the wave equation for a TM wave and obtain all the field components in a rectangular waveguide.
   b) Calculate the "wider" dimensions of a rectangular waveguide operating at 10GHz in TE_{10} mode and has wave impedance 410 ohms.

2. a) An air filled rectangular cavity has following dimensions a=4cm, b=2cm and c=5cm. Designate the first five TE and TM modes of oscillations. Find their resonant frequencies.
   b) What is microstrip line? How does its characteristic impedance change with change in width to height ratio? Give a reason for using lower dielectric constant substrate in place of alumina at higher microwave frequencies.

3. a) In a lossless H-plane tee, a microwave signal of 100mW is fed into one of the collinear arms, say 1. Find the power delivered to the other ports 2 and 3 when these are terminated in the matched loads.
   b) Derive the scattering matrix of a magic tee.

4. a) Explain the principle of operation of an isolator.
   b) Prove that any lossless matched, non reciprocal three port microwave junction is a perfect three port circulator.

5. a) Describe the operation of Reflex Klystron. Find out relationship between accelerating voltage and repeller voltage.
   b) Explain the operation of a two cavity klystron amplifier. Derive expression for bunched beam current and efficiency.

6. a) Describe the principle of operation of a travelling wave tube. List various applications of TWT. What is the most important advantage of TWT over the klystron amplifier?
   b) Explain how amplification is achieved in a Magnetron with neat sketch.

7. a) What is Gunn Effect? Explain the working of a Gunn diode oscillator.
   b) Explain the operation, construction and application of TRAPATT diode.

8. a) How would you measure VSWR in laboratory?
   b) Explain the characteristic of various types of bolometers available for the measurement of low microwave power.

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R-11 / R-13

Code: 1G361

III B.Tech. II Semester Supplementary Examinations May 2017

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions
All Questions carry equal marks (**14 Marks** each)
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1.	a)	Explain the fabrication of Bi-CMOS technology with relevant diagrams.	10M
	b)	List the differences between CMOS and Bipolar technologies.	4M
2.	a)	Derive the relationship between pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter(Zpu/Zpd)	8M
	b)	Draw the transfer characteristics of CMOS inverter and explain.	6M
3.	a)	Draw the stick diagram and mask layout for CMOS NAND gate and CMOS NOR gate.	10M
	b)	Find the scaling factor for Gate area (Ag) and gate Capacitance (Cg).	4M
4.	a)	Derive an expression for sheet resistance (Rs) and apply the concept for calculation of sheet resistance for CMOS inverter.	8M
	b)	Draw the circuit diagram of inverting type NMOS super buffer and explain.	6M
5.	a)	With a neat diagram, explain 4-bit barrel shifter.	7M
	b)	Explain 4-bit Serial- parallel multiplier with a neat diagram.	7M
6.	a)	Explain Programmable Logic Array (PLA) with an example.	8M
	b)	Draw a neat diagram of simple FPGA logic cell and explain.	6M
7.		Explain the concept of design verification tools used in VHDL synthesis tools.	14M
8.	a)	Explain briefly fault models and IDDQ testing.	8M
	b)	With a neat diagram, explain sequential logic testing.	6M

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