Hall Ticket Number :										

R-13

Code : 1G361

III B.Tech. II Semester Supplementary Examinations February 2021

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

****

1 Write short notes on the following

(a) Ion Implantation 4M

(b) Encapsulation 3M

(c) Lithography 4M

(d) Oxidation 3M

2. Derive the Ids – Vds relationship of MOS transistor in saturated and non-saturated regions 14M

3. a) Explain VLSI design flow with neat sketch 7M

b) Discuss indetail about limitations on scaling 7M

4. Write short notes on

(a) Sheet resistance concept to MOS 7M

(b) Wiring capacitances 7M

5. Explain the following with neat diagrams.

(a) Parity generators 7M

(b) High density memory elements 7M

6. Discuss about the following in detail with neat diagrams

(a) CPLDs 7M

(b) PLAs 7M

7. Explain the following

(a) VHDL Synthesis 7M

(b) Design capture tools 7M

8 Write short notes on the following

(a) Design strategies for test 7M

(b) Layout design for improved testability 7M

***