Hall Ticket Number :										

R-11/R-13

Code : 1G361

III B.Tech. II Semester Supplementary Examinations October 2020

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1	a)	What are the additional two layers in BICMOS technology compared to other?	7M
	b)	Briefly discuss the Fick's law of diffusion.	7M
2.	a)	Explain with neat diagrams about various forms of pull up's	8M
	b)	Explain n MOS inverter with neat circuit diagram	6M
3.	a)	Design a layout diagram for the PMOS logic $Y=(AB+CD)^1$	7M
	b)	Discuss the design rules for wires (orbit 2µm CMOS)	7M
4.		Write short notes on	
		(a) Sheet resistance concept to MOS	7M
		(b) Wiring capacitances	7M
5.	a)	Write short notes o Zero/ One detectors	7M
	b)	Design a magnitude comparator based on the path operators.	7M
6.	a)	Write briefly about channeled gate arrays.	7M
	b)	Implement 2-bit comparator using PROM	7M
7.		Explain the concept of design verification tools used in VHDL synthesis tools.	14M
8	a)	Explain briefly fault models and IDDQ testing.	7M
	b)	With a neat diagram, explain sequential logic testing.	7M

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