Hall Ticket Number :										

R-11 / R-13

Code: 1G361

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2019

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer any **five** questions

All Questions carry equal marks (**14 Marks** each)

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1. a) What are the additional two layers in BICMOS technology compared to other?
   b) Briefly discuss the Fick's law of diffusion.
2. a) What are the various forms of pull-up available for an inverter? Explain them with neat sketch.
   b) Derive an expression for the threshold voltage of a MOS transistor.
3. a) Explain the principles of scaling in MOS transistor.
   b) Why design rule check is employed? Discuss
4. Describe how to overcome the problem of driving large capacitive loads.
5. a) With a neat diagram, explain the 4 X 4 array multiplier.
   b) Describe the design of parity generator with a neat sketch.
6. Explain the features of FPGA and CPLD.
7. a) What is meant by synthesis? List and explain steps involved in synthesis.
   b) Explain different types of simulations.
8. a) Explain the ad-hoc test technique applied to a counter.
   b) Describe the chip level test techniques.

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