	Hall	Ticket Number :	
C	ode	: 4G264	4
-		III B.Tech. II Semester Supplementary Examinations May 2019 <b>Power System Operation and Control</b> (Electrical and Electronics Engineering)	
٢	-	Marks: 70 Inswer all five units by choosing one question from each unit ( 5 x 14 = 70 Mark	
1.	a)	UNIT–I Explain the following	
		<ul> <li>incremental fuel rate curves,</li> <li>ii) Input–Output operational characteristics of thermal plant.</li> <li>iii) Input–Output operational characteristics of Hydro power plant</li> </ul>	9M
	b)	Incremental fuel cost in Rs/MWh for a plant consisting of two units are $dc1/dPG1 = 0.2PG1 + 40$ , $dc2/dP/G2 = 0.25 PG2 + 30$ , find the savings in fuel cost in Rs/hr for the optimal scheduling of a total load of 130 MW as compared to equal distribution of the same load between the two limits.	5M
		OR	
2.	a)	Derive the mathematical determination of optimal allocation of total load among different units.	8M
	b)	The fuel cost of two units are given by $C1 = 0.1 PG^21 + 25 PG1 + 1.6 Rs/hr$ $C2 = 0.1 PG^22 + 32 PG2 + 2.1 Rs/hr$ If the total demand on the generators is 250 MW, find the economical load distribution of the two units.	6M
3.	a)	UNIT-II Explain the hydro- thermal scheduling	6M
	b)	Write about incremental production costs for hydro power plants	4M
	c)	Write classical methods for economic operation of systems plants. OR	4M
4.	a)	A Two-plant system that has a thermal station near the load center and a hydro- power station at a remote location is shown in fig(1). The characteristics of both stations are: $C_1 = (26 + 0.045PG_T)PG_T \dots Rs/hr$ $W_2 = (7 + 0.004PG_H)PG_H \dots m3/s$ and $\Upsilon_2 = Rs. 4 \times 10^{-4} / m^3$ The transmission loss coefficient B <sub>22</sub> =0.0025MW <sup>-1</sup> . Determine the power generation at each station and power received by the load when $\lambda$ =65 Rs/MWh	



Fig 1 Two Plant System

b) Explain optimal power flows.

8M 6M

		UNIT–III								
5.	a)	Derive the transfer function of a single area system with a block diagram.	8M							
	b)	Explain the flat frequency control.	6M							
		OR								
6.	a)	Explain Turbine-speed governing system with a neat diagram?	8M							
	b)	Explain the modeling of excitation systems?	6M							
7.	a)	UNIT-IV Explain the LFC of an Isolated power system.	8M							
	b)	) Two Turbo-alternators rated for 110 MW and 210 MW have governor droop characteristic of 5% from No load to Full load. They are connected in parallel to share a load of 250 MW. Determine the load shared by each machine assuming								
		free governor action.	6M							
		OR								
8.		Explain LFC of a Two area system in both uncontrolled case and controlled case.	14M							
9.	a)	Describe the effect of connecting series capacitors in the transmission system.	6M							
	b)	Explain over voltages on sudden loss of loads.	4M							
	c)	List out various loads which require compensation.	4M							
		OR								
10.		Briefly write about any three of the following								
		a) Shunt compensator								
		b) Thyristor controlled reactor								
		c) Thyristor switched capacitor								
		d) Series compensator								
		e) Unified power flow controller.	14M							
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С	coc	de: 4G465							
		III B.Tech. II Semester Supplementary Examinations May 2019							
		Computer System Architecture							
		(Electrical & Electronics Engineering)							
	-	x. Marks: 70 ver all five units by choosing one question from each unit ( 5 x 14 = 70 Marks ) ********							
		UNIT–I							
а	a)	Name four main components of a computer and give their functions.							
b	)	Describe a single bus structure with a suitable diagram.							
		OR							
а	a)	Describe an error detection circuit for transmission of a 3-bit message using odd parity bit.							
b	p) Perform the subtraction with the following unsigned decimal numbers by taking the 10								
		complement of the subtrahend.							
		i) 6255 – 1425 ii) 1754 – 8646 iii) 24 – 105 iv) 1357 – 240							
	. \	UNIT-II							
	a)	What is meant by micro operation? Explain arithmetic micro operations in detail.	1						
C	)	Discuss the operation of 4-bit Binary Incrementer with neat diagram. OR							
а	a)	Explain fetch and decode operations with a neat diagram.	1						
b	)	Define interrupt. Explain BSA instruction							
		UNIT–III							
а	a)	What is a control unit? Explain control memory with a block diagram?							
b	<b>)</b> )	Analyze Booths multiplication algorithm with example?							
		OR							
а	a)	Explain addition and subtraction with signed magnitude data?							
b	<b>)</b> )	What are the major components of CPU? Explain the Register Organization with a block							
		diagram?							
	. \	UNIT-IV							
	a)	Predict the usage of daisy chaining with neat diagram.							
Ľ	)	What is DMA? What is the need for DMA? Explain the working of DMA. Also, mention its advantages.							
		OR							
a	a)	Summarize the types of Mapping Techniques used in the usage of Cache Memory?							
	,	Explain							
b	<b>)</b> )	Discuss Block diagram of Associative Memory with suitable example.							
		UNIT-V							
а	a)	Explain in detail instruction pipeline							
b	<b>)</b> )	What are the characteristics of multiprocessors?							
		OR							
а	a)	Compare and contrast tightly coupled and loosely coupled multiprocessor.							
		Explain about multi stage memory inter connection structure.	-						

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Code: 4GA61					1	1	1	1		1	1	I	R-14
III B.Tech. II Semester Supplementary Examinations May 2019													
Managerial Economics and Financial Analysis													
( Common to EEE & CSE ) Max. Marks: 70 Time: 3 Hours													
Answer all five units by choosing one question from each unit (5 x 14 = 70 Marks)													
	UNIT–I												
1.	Define mana	ageria	al ec	onon	nics?	Ехр			e an	d sco	pe.		
0			•				OR						
2.	What is dem to the law?	hand	? Sta	ite ai	nd e>	cplair	n law	of d	ema	nd. A	Are th	iere ar	iy exceptions
							<b>T</b> _						
3.	How cost ou	out-put relationship helps the entrepreneurs in expansion decisions. <b>OR</b>											
4.	Discuss the	econ	omic	ne an	d die	- 000			fees	lo in	data	;1	
4.	DISCUSS ITE	ecoi		s an	u uis Г		IT–II		1 300		uela		
5.	Evaluate sol	e tra	der f	orm	L of or								
		0 110				garni	OR						
6.	a) Features of perfect market												
	b) market s	kimn	ning										
	c) penetrat	ion p	ricin	g	F								
							IT–IV						
7.	acquiring a f	ixed	cost				ning t	to ac	com	pany	whic	ch is c	onsidering of
	Rate of retur			•	-		. 400	00					
	Project A :		or th 5 ye	-	posa		5 4ZU	000					
	Each year A		•		nnual	cas	n infl	ow F	Rs 14	000	cons	tant)	
	Project B: co	-								·	L. C.	,	
		Life	5 ye	ears									
	Avg after tax	k ann	ual c	ash	inflo	N		(EAF					
								YEA					
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	Determine N	5 year Rs 10000 Determine NPV Which projects do you recommended.											
	Determine N	<b>u</b> v v	/////0	n pic	jecia	uu j			inter	iucu.			
8.	Explain capi	tal bi	udge	ting t	echr Г	-			ranta	ges,	disa	dvanta	iges.
9.	Briefly discu	<u> </u>		ntina			V_TI		anti	י פתר	vith o	vomnl	<b>A</b> S
Э.		ss al	Juli	ung	CONC	epis			GIII			латтрі	03.
10.	Write basics examples.	s of a	acco	unts	and	class	-		acc	ount	s det	oit, cre	dit rules with

ŀ	Hall <sup>-</sup>	Ficket Number :										
Co	ode:	4G263	4									
		III B.Tech. II Semester Supplementary Examinations May 2019										
		Microprocessors and Microcontrollers										
		( Electrical & Electronics Engineering) Marks: 70 Time: 3										
		time: 3. Answer all five units by choosing one question from each unit ( 5 x 14 = 70 Marl										
		*****										
1.	a)	<b>UNIT-I</b> Draw the pin diagram of 8086 microprocessor and explain the functions of the										
••	u)	following pins.										
		(i) ALE (ii) NMI (iii) INTR (iv) HOLD (v) HLDA (vi) BHE (vii) LOCK	8M									
	b)	What is a procedure? What are different types of procedures in 8086? Discuss										
		each type of procedure with examples.	6M									
2.	a)	<b>OR</b> Distinguish between maximum and minimum modes of operation of 8086.	6M									
۷.	a) b)	What do you mean by addressing mode? What are the different addressing modes	OW									
	D)	supported by 8086? Explain each of them with suitable examples.	8M									
		UNIT-II										
3.	a)	Draw the functional block diagram of 8253 programmable interval timer/counter										
		and explain its modes of operation.	7M									
	b)	Describe the interfacing of D/A converter to 8086 microprocessor with a neat sketch.	7M									
		OR	7 111									
4.	a)	Explain the A/D converter interface to 8086 microprocessor.	7M									
	b)	Interface an Analog to Digital converter ADC with an 8086 microprocessor using										
		8255 ports. Use port A of 8255 for transferring digital data output of ADC to the										
		CPU and port C for control signals. Assume that an analog input is present at input 5 of the ADC and a clock input of suitable frequency is available for ADC. Draw the										
		schematic and write the required assembly language program.	7M									
		UNIT–III										
5.	a)	Discuss about EPROM interfacing with 8086 microprocessor.	6M									
	b)	What are the important features of 8257 DMA controller. Describe the internal										
		architecture and signal description for the same. OR	8M									
6.	a)	Explain the procedure to interface 8257 with 8086. Draw the interfacing diagram										
		and explain.	7M									
	b)	Explain the functions of the following signals of 8257: (i) $\overline{IOR}$ (ii) $\overline{IOW}$ (iii) HRQ										
		(iv) HLDA (v) $\overline{MEMR}$ (vi) $\overline{MEMW}$ (vii) TC (viii) AEN (ix) ADSTB (x) MARK	7M									
		UNIT-IV										
7.	a)	Draw the internal architecture of the 8251 USART and explain each block.	8M									
	b)	Why the synchronous serial data communication much more efficient than	014									
		asynchronous serial data communication explain in detail. OR	6M									
8.	a)	Interface 8251 with 8086 at address 40H. Initialize it in asynchronous transmit										
		mode, with 7 bit character size, baud rate factor 16, one start bit, one stop bit, even										
		parity enable. Further transmit a message "BEST OF LUCK" in ASCII from to a modem?	7M									
	b)	Draw the functional block diagram of 8259 programmable interrupt controller and	7 111									
	D)	explain its operation.	7M									
		UNIT-V										
9.	a)	Explain internal and external memory organization of 8051.	7M									
	b)	Explain the following pins of 8051:	<b></b> -									
		(i) AD <sub>0</sub> - AD <sub>7</sub> (ii) T <sub>0</sub> and T <sub>1</sub> (iii) INT0 and INT1 (iv) TxD and RxD	7M									
10.	a)	<b>OR</b> Explain the procedure for interfacing of DC motor with 8051 microcontroller.	7M									
	b)	Discuss the various modes of operation of timer in 8051 microcontroller.	7M									
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			,		0	*****		ι. Ι	,	
		_				UNIT-I				
1.	a)	Form z-bu	s and y	y-bus r	natrix foi	r the following	syst	em		
			(1)		2	3				
						11	7			
				<i>j</i> 0.2		ii j0.08	2 _			
		<i>j</i> 0.1 <b>ξ</b>					<i>3 j</i> 0.	1		
		÷				-	<u>∣</u> =			7N
	b)		•			mpendence fo		and admittane	ce form with	
		network el	ement	repres	entation	and expressi	on			7N
2.	a)	Consider		ar evet	om notu	OR	ant '	3 bue and fi	nd y-bus matrix	
۷.	a)	using sing		-			asi .		iu y-bus matrix	7N
	b)					twork shown b	below	/		
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		1000		2Ω 、	2 Ω	$\mathfrak{Z}^{1\Omega}$				
		7				Γ				
				0	)					7N
						UNIT-II				
3.	a)	The follow	ing is t	he sys	tem data	a for a load flo	w so	lution:		
			the v	oltages	s at the	end of first	iterat	ion using ne	ewton Raphson	
		method.								
							٦		E DATA	
				Load	data		_	Bus code	Admittance 2-j8	
		BUS CODE	Р	Q	V	REMARKS		1-2	2-jo 1-j4	
		1	_	-	1.06	SLACK	_	2-3	0.66-j2.66	
		2	0.5	0.2	1+j0	PQ	-	2-4	1-j4	
		3	0.4	0.3	1+j0	PQ		3-4	2-j8	
		-	0.0	0.4	1.:0			5-4	2-j0	1014

10M

4M

7M

b) Compare the Gauss-Seidel method, Newton Raphson method for load flow solution

4

0.3

0.1

1+j0

OR

PQ

- 4. a) Write an algorithm for the load flow solution using NR method polar co-ordinates 7M
  - b) Explain why load flow studies are performed and its significance in power system analysis & discuss about the classification of buses

6M

7M

7M

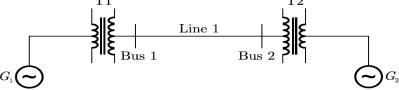
6M

6M

## UNIT-III

5. a) Draw the impedance diagram for the power system shown in the figure below, the specifications of the components are the following :

G1: 25 kV, 100 MVA, X = 9% G2: 25 kV, 100 MVA, X = 9% T1: 25 kV/220 kV, 90 MVA, X = 12% T2: 220 kV/25 kV, 90 MVA, X = 12% T1



Line 1: 200 kV, X = 150 ohms

Choose 25 kV as the base voltage at the generator G1, and 200 MVA as the MVA base.

 b) Derive the expression for the fault current, when an unloaded alternator subjected to single line to ground fault.
 8M

## OR

- a) The voltages across a 3-phase load are V<sub>a</sub> = 300 V, V<sub>b</sub> = 300∠- 90° V and V<sub>c</sub> = 800 ∠ 143.1° V respectively. Determine the sequence components of voltages. Phase sequence is abc.
  - b) A 500 MVA, 50 Hz, 3-phase turbo-generator produces power at 22 kV. Generator is Y-connected and its neutral is solidly grounded. It Sequence reactance's are X1 = X2 = 0.15 pu and X0 = 0.05 pu.It is operating at rated voltage and disconnected from the rest of the system (no load). Find the magnitude of the sub-transient line current for single line to ground fault at the generator terminal

7. a) Derive the expression for maximum steady state power 8M b) Explain methods to improve steady state stability limit 6M OR a) Write short notes on following 8. Power angle diagram i. ii. Steady state stability limit iii. Synchronizing power coefficient 10M b) List the assumptions used in deriving the power angle equation 4M

- 9. a) Explain the effect of fault clearing time on stability
  - b) Derive the expression for critical clearing angle and time when a 3 phase fault occurs on the transmission line
     8M

OR

- a) Explain equal area criterion in case of "sudden loss of one parallel lines" for analyzing transient stability? What happens if mechanical input is larger than maximum power transfer capability after above fault condition occurs?
   8M
  - b) Explain the methods to improve transient stability analysis