Hall	Ticke	et Number :	
Code:	4 <b>G</b> 4	65 R-14	
		ech. II Semester Supplementary Examinations Nov/Dec 2018 Computer System Architecture ( Electrical and Electronics Engineering)	
Max. Ar			Jrs
1.	a)	Describe with neat sketch the functional units of computers.	7M
	b)	Explain in brief complements in data representation.	7M
	,	OR	
2.		Convert the following i. $(756)_{10} = (?)_8$ ii. $(175)_{16} = (?)_{10}$ iii. $(1362)_8 = (?)_2$ iv. $(1110101)_2 = (?)_{10}$ v. $(F3A7C2)_{16} = (?)_8$	14M
3.	a)	How information transfer from one register to another register? Explain.	7M
	b)	List the basic computer instructions. Sketch the basic computer instructions.	7M
		OR	
4.	a)	Describe in brief instruction cycle.	7M
	b)	With neat sketch explain bus system for four registers. UNIT-III	7M
5.		List and explain instruction formats in brief.	14M
		OR	
6		List and explain addressing modes. UNIT-IV	14M
7.	a)	Explain control memory with block diagram.	7M
	b)	Draw the block diagram for selection of address for control memory.	7M
		OR	
8.	a)	Describe the symbolic microinstructions.	7M
	b)	What is the need of decoding of microoperations fields? Explain.	7M
9.	a)	Explain arithmetic pipeline with an example.	7M
	b)	What is cache coherence? Explain.	
		OR	
10.	a)	Describe Crossbar switch interconnection structure.	7M
	b)	Briefly explain the parallel processing.	7M
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Hall T	icke	t Number :								
Code:		R-14								
		ech. II Semester Supplementary Examinations Nov/Dec 2018								
		Microprocessors and Microcontrollers								
		(Electrical & Electronics Engineering)								
Max. I An	-	time: 3 Hou r all five units by choosing one question from each unit ( 5 x 14 = 70 Marks ) ********	Jrs							
		UNIT–I								
1.	a)	Distinguish minimum mode and maximum mode of operation								
	b)	Explain the instruction format of 8086µP with an example	6M							
		OR								
2.	a)	Advantages of procedures used in 8086 $\mu$ P? Illustrate the syntax of it.	8M							
	b)	List out the assembler directives used in 8086µP.	6M							
3.	a)	UNIT–II Describe about memory mapped I/O Interfacing.	7M							
0.	b)	Describe the stepper motor interfacing with 8086 $\mu$ P.	7M							
	~)	OR								
4.	a)	Describe the A/D converters interfacing with 8086 $\mu$ P.	7M							
	b)	Write an assembly language program to interface 8255 in mode-0 with 8086.	7M							
		UNIT–III								
5.	a)	Explain about 4KB of RAM Memory interfacing with 8086.	7M							
	b)	Explain about modes of 8257.	7M							
0	- )	OR	71.4							
6.	a) Þ	Illustrate the basic structure of SRAM and DRAM cells	7M							
	b)	Need for DMA? Explain the master and slave modes of DMA.	7M							
		UNIT–IV								
7.	a)	Describe 8259 PIC architecture.	7M							
	b)	Describe TTL to RS232C and RS232C to TTL conversion.	7M							
	,	OR								
8.	a)	Describe 8251 USART architecture.	7M							
	b)	Describe Vector interrupt table of 8086 µP.	7M							
		UNIT-V								
9.	a)	Explain about RAM organization in $8051 \mu$ C.	7M							
	b)	Explain about Timer/Counters of 8051µC.	7M							
40	<b>c</b> )	OR	71.4							
10.	a) b)	Draw the pin diagram 8051µC.	7M 7M							
	b)	Describe the addressing modes 8051µC.	7M							

Hall Ti	cket Number :										1
Code:	4C-261		I I.	_			1		R	R-14	
	B.Tech. II Ser	nester (	Supple	menta	rv Fx	ami	nati	ons	Nov/Dec 2	018	
			Power		•			0110			
			rical & E	-		-		g)			
Max. I	Marks: 70	·				0		0,	Time	: 3 Hours	
Ar	iswer all five unit	ts by cho	osing on	e questi		m eq	achι	unit (	5 x 14 = 70 M	arks )	
					IIT–I						
1. a)	Write the mathe	ematical r	nodelina	L		wers	svste	m ele	ements.		7
b)	Starting from th		-		-		•			equal to	
- /	the sum of adm	•	•			•				•	
	the negative of	the admit	ttance di	ectly cor	nnecte	ed be	twee	n the	buses.		7
				C	DR						
2.	For the network	shown ii	n fig belo	ow, form	ZBUS	usin	g ste	p by	step algorithm	า.	
				je	). <b>3</b>						
			a					3			
			- <u>E</u>	j0.2	Ø	JO.1	<u>-</u>				
			j1.2	l			J1.5	5			
				P2	0	2	5				14
				UN	IT-II						1-1
3. a)	Write an algorit	hm for Ga	auss-Sei			netho	d inc	ludin	g PV buses.		8
b)	What are the d								•	, explain	
,	each one of the	-	•							•	6
				C	DR						
4.	For the power while loads are	e at bus	es 2,3	and 4.	The va	alues	of re	eal ar			

while loads are at buses 2, 3 and 4. The values of real and reactive powers are listed in table 1. All buses other than slack bus are of P-Q type. Line data are given in table 2. Assuming a flat voltage start, determine the voltage magnitudes and the phase angles at the three buses using G- S(Gauss-Seidel) method for first iteration.

Table 1.	Βι	is data				
Bus Pi		i	Qi	Vt	Type of bus	
1		-		1.05 0	Slack	
2	2 -0.45 3 -0.51		-0.15		PQ	
3			-0.25		PQ	
4	4 -0.		-0.3		PQ	
Table 2.	Li	ne data				
Line No. Bus		Bus Co	de(p-q)	Line Imped	lance	
1		1-2		0.08+j0.2		
2		1-4		0.05+j0.1		
3		2-3		0.04+j0.12		
4		3-4		0.04+j0.14		

14M

## UNIT–III

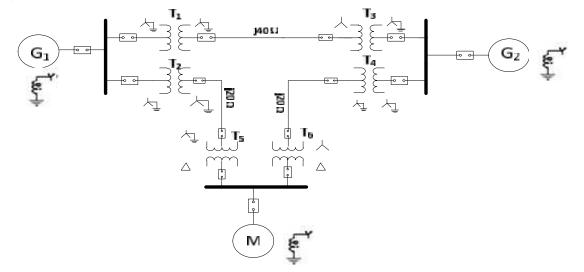
5. a) Draw the reactance diagram for the power system shown in below fig. The ratings of generator, motor and transformers are given below. Neglect resistance and use a base of 50MVA, 138KV in the 40 line.

Generator G<sub>1</sub>: 20 MVA,18KV,X<sup>"</sup>=20%;

Generator G<sub>2</sub>: 20 MVA,18KV,X"=20%;

Synchronous Motor: 30MVA, 13.8KV, X<sup>"</sup>=20%;

- 3-phase Transformer: 20MVA, 138KV/20KV, X=10%;
- 3-phase Transformer: 20MVA, 138KV/20KV, X=10%;



b) Three phase voltages across a certain unbalanced  $3\Phi$  load are given as  $E_R = 176$ -j132;  $E_Y = -128$ -j96 and  $E_B = -160$ +j100. Find Positive, Negative and Zero sequence components of voltages.

OR

- 6. a) Explain interconnection of sequence networks for a LL-G fault in power system network with necessary equations.
  - b) A 25MVA, 11kV Synchronous Generator has positive, negative and zero sequence reactances of 12%, 12% and 8% respectively. The generator neutral is grounded through a reactance of 5%. A Single line to Ground fault occurs at the generator terminals. Determine fault current and line to line voltages. Assume that the generator is unloaded before fault.

- 7. a) Prove that maximum power transfer can be achieved when X= 3 R. 7M
  - b) Explain various methods to improve Steady State Stability.

## OR

- 8. a) Derive the expression for the steady state stability limit.
  - Explain the synchronizing power coefficient and analyze the system stability using power angle curve.
     7M

9. a) Explain various methods of improving transient stability.

b) Derive the Swing equation of a Synchronous machine.

## OR

- 10. a) With the help of Equal area criterion for one machine connected to Infinite bus, derive the expressions for critical clearing angle and critical clearing time.
  - b) A 50HZ generator is delivering 50% of the power that is capable of delivering through a transmission line to an infinite bus. A fault occurs that increases the reactance between generator and infinite bus 500% of the value before fault. When the fault is isolated the maximum power that can be delivered is 75% of the original maximum value. Determine the critical clearing angle for the condition delivered.

7M

7M

7M

8M

6M

7M

7M 7M

8M

6M

	R-14
	Code: 4G264
	III B.Tech. II Semester Supplementary Examinations Nov/Dec 2018 <b>Power System Operation and Control</b>
	(Electrical and Electronics Engineering)
	Max. Marks: 70 Time: 3 Hours
	Answer all five units by choosing one question from each unit ( 5 x 14 = 70 Marks )
	********* UNIT–I
a)	Explain the significance of equality and inequality constraints in the economic
u)	allocation of generation among different plants in a system
b)	A system consists of three generating plants with fuel costs of:
,	$C_1=0.04P_1^2+20P_1+230 \text{ Rs./h}$
	$C_2=0.06P_2^2+18P_2+200 \text{ Rs./h}$
	$C_3=0.15P_3^2+15P_3+180 \text{ Rs./h}$
	Determine the optimum sharing of a total load of 180MW for which each plant
	would take up for minimum input cost of received power in Rs/MWh. OR
a)	What are Loss coefficients? Derive the expressions for Loss coefficients of a two generator system.
b)	Draw the flow chart for obtaining optimal scheduling of generating units by neglecting the
	transmission losses.
a)	Explain problem formation and solution procedure of optimal scheduling for hydro thermal plants.
b)	A load is fed by two plants, one is thermal and other is a hydro plant. The load is located near
	the thermal plant. The characteristics of the plants are
	$F_T = 0.04P_T^2 + 25PT + 20 Rs./hr; W_H = 0.0012P_H^2 + 7.5P_H m3/Sec;$
	$x_{H}=2.5X10^{-3}$ Rs./m <sup>3</sup> . Determine the power generation of both plants and load connected, when
	$\lambda = 20$ Rs./ MWh.
a)	Obtain the modeling of hydro turbine and draw its block diagram.
b)	With the help of a flow chart, explain the dynamic programming method in unit commitment.
a)	Explain speed governing mechanism. Develop its block diagram.
b)	Develop the block diagram of Generator and load.
、	OR
a)	Why is it necessary to maintain constant frequency and voltage profiles in a power system network? Explain.
b)	Draw and explain the Block diagram of IEEE type-1 excitation system.
5)	
a)	Draw the block diagram of single area Load frequency control system. Explain the terms in it.
b)	Two generators of rating 125 and 250MW are operated with droop characteristics of 4% and 5%
	respectively from no load to full load. Find the load sharing by each generator if a load of 300MW
	is connected across the parallel combination of those generators.
a)	Show that steady state frequency deviation in a single area LFC is reduced to zero if the PI
α,	controller is reduced.
b)	Discuss the importance of combined load frequency control and economic dispatch control with
	a neat block diagram.
a)	What do mean by compensation of a line? Discuss briefly different methods of compensation.
b)	Explain what you mean by loadability of overhead lines and discuss loadability characteristic of these lines.
	OR
a)	What is sub synchronous resonance condition? How is it handled in electrical network?
b)	A 35 kW induction motor has power factor 0.85 and efficiency 0.9 at full load, power factor 0.6
	and efficiency 0.7 at half-load. At no-load, the current is 25% of the full-load current and power
	factor 0.1. Capacitors are supplied to make the line power factor 0.8 at half-load. With these capacitors in circuit, find the line power factor at (i) full load, and (ii) no-load.