Hall Ticket Number :										

R-14

Code: 4G465

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2019

Computer System Architecture

(Electrical and Electronics Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Name four main components of a computer and give their functions 7M

   b) Describe a single bus structure with a suitable diagram 7M

OR

2. What is overflow and underflow ,what is the reason if the computer is considered as infinite system do we still have the problem justify answer 14M

UNIT–II

3. a) What are the various shift micro operations explain them in brief 7M

   b) Perform the logic AND OR and XOR with the two binary strings 10011100 and 10101010 7M

OR

4. a) Explain fetch and decode operations with neat diagram 7M

   b) What is an interrupt explain about BSA instruction 7M

UNIT–III

5. What are the major components of CPU explain stack organization with a block diagram 14M

OR

6. a) Explain with the help of diagram the selection of address for control memory 7M

   b) Discuss in brief about the applications of microprogramming 7M

UNIT–IV

7. What is DMA and need of DMA explain the working of DMA and mention its advantages 14M

OR

8. Summarize and explain the types of mapping techniques used in the usage of cache memory 14M

UNIT–V

9. a) What are the characteristics of multiprocessor explain in brief 7M

   b) Compare and contrast tightly coupled and loosely couples multiprocessor 7M

OR

10. What is the pipeline name the two pipeline organization explain about arithmetic pipeline with the help of example 14M

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Hall Ticket Number :										

R-14

Code: 4G263

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2019

Microprocessors and Microcontrollers

(Electrical & Electronics Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) With a neat diagram, explain the internal architecture of 8086 microprocessor. 8M
   b) What is an assembler directive? Explain any five assembler directives with examples. 6M

OR

2. a) Write an assembly language program in 8086 to arrange the given 16-bit numbers in lowest to highest order. 7M
   b) Draw the register organization of 8086 and explain typical applications of each register. 7M

UNIT–II

3. a) Explain the 8255 programmable peripheral interface and its operating modes with a neat functional block diagram. 7M
   b) Explain the interfacing procedure of an 8-bit DAC with 8086 microprocessor. 7M

OR

4. a) Discuss about I/O mapped I/O and memory mapped I/O. Write a comparison between I/O mapped I/O and memory mapped I/O. 6M
   b) Draw and explain the stepper motor interface to 8086 and write small program to rotate stepper motor in clock wise and anticlockwise direction 8M

UNIT–III

5. a) Explain the need for DMA data transfer? Draw and discuss the architecture of 8257. 7M
   b) Explain how static RAM is interfaced to 8086. Give necessary interface diagram assuming appropriate signals and memory size. 7M

OR

6. a) Explain the features of static RAM and dynamic RAM. Give the comparison between these two. 7M
   b) What are the advantages of DMA controlled data transfer over interrupt driven or program controlled data transfer? Why are DMA controlled data transfers faster? 7M

UNIT–IV

7. a) Explain with a neat diagram the working of 8251 PCI. 8M
   b) Draw the interface circuits for data conversion from
   (i) TTL to RS232C and (ii) RS232C to TTL 6M

OR

8. a) Describe the purpose of 8086 interrupt vector table. 6M
   b) With a neat schematic, explain the interfacing of 8259 with 8086 microprocessor. 8M

UNIT–V

9. a) Discuss the features of 8051 microcontroller and explain its operation with the help of a block diagram. 7M
   b) Explain the various instruction set of 8051 microcontroller. 7M

OR

10. a) What are the addressing modes of 8051 microcontroller? Explain each addressing mode with an example. 6M
    b) Discuss about the salient feature of ARM (Advanced RISC Machines) processors 4M
    c) Explain the different types of interrupts and their priorities in 8051. 4M

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Hall Ticket Number :										

R-14

Code: 4G261

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2019

Power System Analysis

(Electrical and Electronics Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

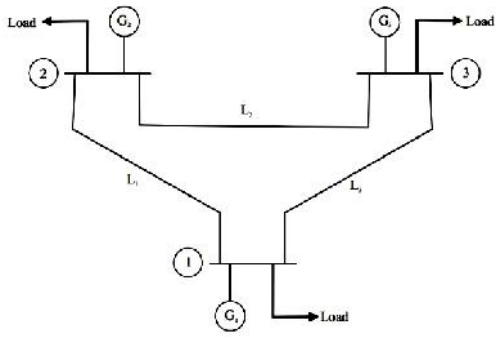
1. a) Write Z bus building algorithm 6M

   b) Derive the expression for bus admittance matrix Ybus in terms of primitive admittance matrix and bus incidence matrix 8M

OR

2. a) Write the procedure for the modifications of Z bus matrix for Network Changes 4M

   b) Consider the power system shown. Each generator and the line impedance of j0.2 pu and j0.5 pu respectively. Neglecting line charging admittances, form y bus matrix using direct inspection and singular transformation



10M

UNIT–II

3 The following is the system data for a load flow solution:

LINE DATA	
Bus code	**Admittance**
1-2	2-j8
1-3	1-j4
2-3	0.66-j2.66
2-4	1-j4
3-4	2-j8

Load data				
BUS CODE	**P**	**Q**	**V**	**REMARKS**
1	-	-	1.06	SLACK
2	0.5	0.2	1+j0	PQ
3	0.4	0.3	1+j0	PQ
4	0.3	0.1	1+j0	PQ

Determine the voltages at the end of first iteration using Gauss-Seidel method. 14M

OR

4. a) With a neat flow chart explain the load flow solution by Guass-seidal method 7M

   b) Explain

      I. Decoupled load flow and

      II. Fast decoupled load flow methods 7M

UNIT–III

5. a) Derive the fault current equation for double line to ground fault for an unloaded alternator 8M

   b) The line currents in a 3-phase supply to an unbalanced load are respectively $I_a = 10 + j20$, $I_b = 12 - j10$ and $I_c = -3 - j5$ amperes. The phase sequence is abc. Determine the sequence components of currents 6M

OR

6 a) What is meant by per unit quantity? Why per unit method is considered superior to percent method for short-circuit calculations? 4M

   b) A double line to ground fault occurs on phases *b* and *c*, at point *P* in the circuit whose single line diagram is shown Determine the sub transient currents in all phases of machine-1, the fault current and the voltages of machine I and voltages at the fault point. Neglect pre-fault current. Assume that machine-2 is a synchronous motor operating at rated voltage. Both the machines are rated 1.25 MVA, 600 volts with reactance's of $X'' = X2 = 8\%$ and $X0 = 4\%$. Each 3-phase transformer is rated 1.25 MVA, 600 volts delta/4160 volts star with leakage reactance of 5%. The reactance's of transmission line are $X1 = X2 = 12\%$ and $X0 = 40\%$ on a base of 1.25 MVA, 4160 volts

10M

UNIT–IV

7. a) Derive the condition for maximum power transfer can be achieved 7M

   b) What is meant by stiffness of synchronous machine and explain how stability of the system can be understood using synchronizing power coefficient? 7M

OR

8. a) Derive the power angle equation? 7M

   b) Explain methods to improve steady state stability limit also explain the deference between steady state stability limit and transient state stability limit 7M

UNIT–V

9. a) Explain equal area criterion in case of "**sudden change in mechanical input"**? Discuss its application and limitation in the study of power system Stability. 8M

   b) Derive the swing equation explaining symbol of each term used 6M

OR

10. a) Explain the point by point method of solving the swing equation. Compare his method with the equal area criterion method 8M

    b) Explain the methods to improve transient stability analysis 6M

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Hall Ticket Number :										

R-14

Code: 4G264

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2019

Power System Operation and Control

(Electrical and Electronics Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Derive the transmission loss formula of a power generator system. 7M

   b) Consider a Two Bus system in which plant1 and plant2 are connected to each bus and load is connected to bus2.If a load of 125 MW is transmitted from plant1 to the load a loss of 15.625MW in incurred. Determine the generation schedule and the load demand if the cost of received power is Rs.24 /MWhr. The incremental production costs of the plants are:

   dF1/dP1 = 0.025 P1 + 15,

   dF2/dP2 = 0.05 P2 + 20, 7M

OR

2. a) Derive the expression for loss coefficients and state the assumptions made in deriving the same. 7M

   b) Incremental fuel costs in rupees per MWh for a plant consisting of two units are:

   dC1/dPG1 = 0.2 PG1 + 40.0,

   dC2/dPG2 = 0.2 PG2 + 30.0,

   Assume that both units are operating at all times and total load varies from 40MW to 250 Mw and the maximum and minimum loads on each unit are to be 125 and 120 MW respectively. How will the load be shared between the two units as the system load varies over the full range? What are the corresponding values of the plant incremental costs? 7M

UNIT–II

3. a) Write the optimal scheduling of hydro thermal system. 7M

   b) Explain hydroelectric power plant models. 7M

OR

4. A Two-Plant system having a steam plant near the load centre and a hydro-plant at a remote location. The load is 500MW for 16 hours a day and 350 MW, for 8 hours a day. The characteristics of the unit are:

   C1 = 120 + 45 PGT + 0.075 P^2GT,

   W2 = 0.6 PGH + 0.00283 P2GH m^3/s

   Loss co-efficient,B_{22} + 0.001 MW^{-1}

   Find the generation schedule, daily water used by the hydro plant, and daily operating cost of the thermal plant for λ_j = 85.5 Rs./ m^3 - hr 14M

UNIT–III

5. a) With the help of neat sketch, explain about various parts of speed-governing system. 8M

   b) Write about modeling of excitation systems? 6M

OR

6. a) Write the block diagram representation of steam turbines and approximate linear models. 8M

   b) Write about the modeling of governor. 6M

UNIT–IV

7. a) Discuss the merits of proportional plus integral LFC of a system with a neat block diagram. 5M

   b). with a neat block diagram explain dynamic response and the steady state analysis of isolated power system 9M

OR

8. a) Explain Tie-line bias control. 4M

   b) Explain optimal two area load frequency control. 10M

UNIT–V

9. a) Explain about compensated transmission lines? 8M

   b) A 3-Phase 5kW induction motor has a power factor of 0.85 lagging. A bank of capacitor is connected in delta across the supply terminal and power factor raised to 0.95 lagging. Determine the KVAR rating of the capacitor in each phase. 6M

OR

10. a) Write the advantages and disadvantages of different types of compensating equipment for transmission systems? 7M

    b) Discuss the effects of reactors and capacitors in reactive power control. 7M

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