Hall Ticket Number :										

R-14

Code: 4G365

III B.Tech. II Semester Supplementary Examinations May 2018

Digital Signal Processing

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Test the following systems for Linearity, Time Invariant, Stability and Causality
$y(n) = x(n) + 0.5\,x(n-1) + 0.25\,x(n-2)$ 7M

   b) Determine the response y(n), $n \geq 0$ of the system described by the second order difference equation $y(n)-3y(n-1)+4y(n-2)=x(n)+2x(n-1)$ where $x(n)=4^n u(n)$. 7M

OR

2. a) Compute the DFT of the four point-sequence: x(n) = (0 ,1,2,3) 7M

   b) Prove the following DFT properties: Circular Symmetries of a Sequence, Linearity 7M

UNIT–II

3. a) Distinguish between DFT and FFT. 5M

   b) Calculate DFT of the sequence x(n)={1,2,3,4,4,3,2,1} using DIT-FFT algorithm. 9M

OR

4. a) Derive the Radix-2 DIT-FFT algorithm. 7M

   b) Compute 8 point DFT of the sequence x(n)={1/2,1/2,1/2,1/2,0,0,0,0} using DIF-FFT algorithm. 7M

UNIT–III

5. a) Obtain the analog Chebyshev filter transfer function that satisfies the constraints
$1/\sqrt{2} \leq |H(j\Omega)| \leq 1 \quad ; \quad 0 \leq \Omega \leq 2 \qquad |H(j\Omega)| < 0.1 \; ; \quad \Omega \geq 4$ 7M

   b) Bring out the salient features of IIR Structures Direct form–I, Direct form- II 7M

OR

6. a) Compare and contrast IIR and FIR filters. 5M

   b) Explain the Design of FIR digital filters using window techniques. 9M

UNIT–IV

7. a) Discuss Decimation by a factor D. 7M

   b) Explain the concept of Sampling rate conversion by a rational factor I/D. 7M

OR

8. a) Discuss Interpolation by a factor I. 7M

   b) Discuss the Filter Design and Implementation for Sampling rate conversion. 7M

UNIT–V

9. a) Describe spectral analysis of non stationary signals in DSP. 7M

   b) What are the major blocks in Musical sound processing? Explain briefly. 7M

OR

10. a) Explain about Oversampling D/A conversion in signal processing applications. 7M

    b) Write Short notes on applications of Digital signal processing. 7M

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Hall Ticket Number :										

R-14

Code: 4G363

III B.Tech. II Semester Supplementary Examinations May 2018

Microprocessors & Interfacing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Explain the Addressing modes of 8086 processor? Explain the addressing modes of 8086 microprocessor with suitable examples? Assume BX=0158, DI=10A5, Displacement = 1B57, DS=2100 and DS is used as segment register, and then calculate the effective and physical address for the following addressing modes.
(i) Direct (ii) Register Indirect and Register Relative (assume register BX)
(iii) Based Index and Relative based index (assuming register BX). 10M

b) What is the length of instruction Queue in 8086? Discuss the use of Queue. Explain the reason for limiting the length of queue. 4M

OR

2. a) Explain the maximum mode configuration of 8086 microprocessor. Show the timing diagrams for READ and WRITE operations. 10M

b) Write an 8086 Assembly Language Program (ALP) to add a data byte located at offset 0500H in 2000H segment to another data byte available at 0600H in the same segment and store the result at 0700H in the same segment. 4M

UNIT–II

3. a) Explain the internal architecture of 8255 and explain its modes of operation in detail. 10M

b) Interface two 4K X 8 EPROMs and two 4K X 8 RAM chips with 8086 microprocessor. Select suitable maps. 4M

OR

4. a) Interface four 7-segment displays to 8086 microprocessor using 8255 PPI, and write relevant 8086 ALP to display in sequence 8, 0, 8, 6 over the four seven segment displays continuously. 10M

b) Show the interfacing of DAC with 8086 and write relevant assembly language program (ALP) to generate Triangular Waveform 4M

UNIT–III

5. a) Draw the block diagram of 8259 PIC and gives its interrupt priority modes? 10M

b) Distinguish between programmed I/O and Interrupt driven I/O. 4M

OR

6. a) Draw the block diagram of 8253 programmable timer/counter and explain its architecture. 10M

b) Give the sequence of steps that are initiated by 8086 microprocessor, when an interrupt type INTN is executed. 4M

UNIT–IV

7. a) Draw the block diagram of 8251 USART and explain each block. 10M

b) Write about asynchronous and synchronous data transfer schemes. 4M

OR

8. a) With the help of a flowchart, write a Program to transmit 100 bytes of serial data. 10M

b) Name serial communication standards and draw TTL to RS232 & RS232 to TTL conversion circuits. 4M

UNIT–V

9. a) Explain Real and Virtual mode in 80286? Also explain the mapping of virtual memory with physical memory. 10M

b) What are the major architectural advancements in 80386 over 80286? 4M

OR

10. a) With neat diagram, explain the Pentium CPU architecture. 10M

b) List the salient features of Pentium Pro Processors. 4M

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Hall Ticket Number :										

Code: 4G362

R-14

III B.Tech. II Semester Supplementary Examinations May 2018

Microwave Engineering

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Derive the wave equation for a TM wave and obtain all the field components in a rectangular wave guides. 8M

   b) A 10GHz signal is to be propagated through a rectangular waveguide. Calculate the dimensions of the waveguide, guide wavelength and phase velocity, for dominant mode of propagation. 6M

OR

2. a) Draw the EM spectrum and list all the frequency ranges involved in microwave bands. 7M

   b) Differentiate Dominant and Degenerate modes. Explain the significance of Dominant Mode. Also sketch the dominant and degenerate modes for TE and TM modes in a rectangular waveguide. 7M

UNIT–II

3. a) A rectangular-cavity resonator has dimensions of a=5 cm, b=2 cm and d=15cm, compute i) The resonant frequency of the dominant mode for an air-filled cavity. ii) The resonant frequency of the dominant mode for a dielectric-filled cavity of εr=2.56. 8M

   b) Define a reentrant cavity and Mention where it is used? Explain the quality factor of cavity resonator. 6M

OR

4. a) A Circular waveguide operating in the dominant mode at a frequency of 9GHz with maximum field strength of 300V/cm. The internal diameter is 5cm. Calculate the maximum power. 6M

   b) Derive the Field equations for TE mode in circular waveguide. 8M

UNIT–III

5. a) Summarize the operation of magic tee with neat diagram and derive it's S-matrix? 7M

   b) Explain in detail about waveguide irises, tuning screws and posts, waveguide attenuators with neat diagram? 7M

OR

6. a) A Three port circulator has an insertion loss of 1dB, isolation 30 dB and VSWR = 1.5. Find the S – matrix. Also convert a three port circulator into an isolator and derive its S-Matrix. 8M

   b) Identify the various losses in the network. Represent these losses using S-parameters. 6M

UNIT–IV

7. a) A two-cavity amplifier klystron has the following parameters beam voltage Vo= 900V, beam current Io= 30mA, frequency f =8GHz, gap spacing in either cavity d= 1mm, spacing between centers of cavities L=4cm, effective shunt impedance Rsh=40KΩ, determine i)The electron velocity ii)The dc electron transit time iii)The input voltage for maximum output voltage iv)The voltage gain in decibels. 6M

   b) Derive the expression for bunching process, output power and efficiency of reflex klystron? 8M

OR

8. a) Suggest the methods to suppress oscillations in TWT and explain the nature of four propagation constants. 6M

   b) Recall the operation of 8-cavity cylindrical travelling wave magnetron and derive it's hull cutoff voltage? 8M

UNIT–V

9. a) Appraise RWH theory and the various modes of operation of GUNN Diode. 8M

   b) Elaborate different methods of measurement of impedance using microwave bench? 6M

OR

10. a) Draw the block schematic of typical microwave bench and explain the functionality of each block. 7M

    b) Explain the principle of working of IMPATT diode with suitable structure and characteristics. 7M

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R-14

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III B.Tech. II Semester Supplementary Examinations May 2018

VLSI Design

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1 a) Explain the processing steps used in IC fabrication process. 8M

b) List the differences among nMOS, CMOS and BiCMOS. 6M

OR

2. a) Deduce the expressions for drain-to-source current versus drain-to- source voltage relations. 7M

b) Draw and explain the characteristics of nMOS transistor in different modes of operation and its body effect. 7M

UNIT–II

3. a) Explain the color code used for drawing stick diagram for NMOS and PMOS designs. 8M

b) Design the NMOS inverter circuit and explain its operation. 6M

OR

4. a) Determine the pull-up to pull-down ratio for an nMOS inverter driven by another nMOS inverter. 10M

b) What is the need for Stick diagrams? 4M

UNIT–III

5. a) What is meant by sheet resistance R_S? Explain the concept of R_s applied to MOS transistors. 7M

b) Explain the concepts of 'nMOS inverter pair delay' and 'Minimum size CMOS inverter pair delay with necessary circuit diagrams. 7M

OR

6. a) Discuss about area capacitances of MOS layers and give area capacitance calculations with suitable examples. 9M

b) Explain how MOSFETs can be used as switches 5M

UNIT–IV

7. a) Describe the nature of a parity generator and explain its structured design approach. 8M

b) Discuss in detail about the CPLD Design 6M

OR

8. a) Draw and give the design approach for a carry look ahead adder with its structure 8M

b) Write short notes on Standard Cell Based Designs. 6M

UNIT–V

9. a) Define testing. What is the role of testing in VLSI chips? 7M

b) Write short notes on System level test techniques 7M

OR

10. a) Write short notes on Chip level test techniques 7M

b) Explain briefly about design capture tools 7M

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