Hall Ticket Number :										

R-15

Code: 5G366

III B.Tech. II Semester Supplementary Examinations February 2021

Radar Engineering

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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			Marks	CO	Blooms Level
		UNIT–I			
1.	a)	Interpret the Radar range equation with Integration of Radar pulses.	7M	CO1	V
	b)	Find the maximum range of Radar whose transmitted power is 150 KW, cross sectional area of the target is 20 sq. m. The minimum power received is 1mw. The power gain of the antenna used is 950 at the operating frequency of 2GHz.	7M	CO1	I
		OR			
2.	a)	Develop the basic block diagram of RADAR system and Outline its operation.	7M	CO1	III
	b)	Illustrate cross sectional area of the target influences on received signal of Radar system.	7M	CO1	II
		UNIT–II			
3.	a)	Interpret the operation of CW radar with non-zero IF in the receiver with block diagram.	8M	CO2	V
	b)	List the applications of CW radar.	6M	CO2	I
		OR			
4.	a)	Explain the operation of FMCW radar with block diagram.	7M	CO2	II
	b)	Justify, Doppler effect occurs in stationary target or not.	7M	CO2	II
		UNIT–III			
5.	a)	Construct the block diagram of non-coherent MTI radar and explain the operation.	10M	CO3	III
	b)	Identify the limitations of MTI radar performance	4M	CO3	III
		OR			
6.	a)	An MTI radar operates at 5 GHz with PRF of l000 PPs. Find the 3 lowest blind speeds of this radar	7M	CO3	I
	b)	Define Blind Speed and what the use of delay line chancellor.	7M	CO3	I
		UNIT–IV			
7.	a)	Draw the block diagram of conical-scan tracking radar and explain.	10M	CO4	III
	b)	List the limitations of tracking accuracy.	4M	CO4	I
		OR			
8.	a)	Explain about Phase comparison monopulse.	8M	CO4	II
	b)	Distinguish Monopulse tracker with Conical scan tracker.	6M	CO4	IV
		UNIT–V			
9.	a)	List the types of Radar displays.	6M	CO5	I
	b)	Three network units each of 4 dB noise figure and 9 dB, 5 dB and 2 dB gains respectively are cascaded, calculate the overall noise figure of the system.	8M	CO5	III
		OR			
10.	a)	Interpret principle and characteristics of a matched filter.	7M	CO5	IV
	b)	Derive the expression for its frequency response function	7M	CO5	II

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Code: 5G361

III B.Tech. II Semester Supplementary Examinations February 2021

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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			Marks	CO	Blooms Level
		UNIT–I			
1.	a)	Apply fabrication principles to nMOS process with neat diagrams.	8M	1	L3
	b)	Explain oxidation, Photolithography and diffusion	6M	1	L2
		OR			
2.	a)	Describe I_{ds}-V_{ds} relationships of nMOS circuits.	7M	1	L2
	b)	Translate MOS transistor threshold voltage and transconductance (gm).	7M	1	L1
		UNIT–II			
3.	a)	Explain CMOS design rules for wires, contacts and transistors layout diagrams for CMOS inverters.	7M	2	L2
	b)	Prepare the stick diagram and layout diagram for NAND gate using CMOS encoding style.	7M	2	L3
		OR			
4.	a)	Explain the layers NMOS.	7M	2	L2
	b)	Discuss in detail about scaling and derive scaling factors for various parameters	7M	2	L1
		UNIT–III			
5.	a)	Calculate nMOS transistors area of capacitance.	6M	3	L4
	b)	Explain different switch logic used for designing of VLSI circuits?	8M	3	L2
		OR			
6.	a)	Derive an expression for sheet resistance (Rs) and apply the concept for Calculation of sheet resistance for CMOS inverter.	6M	3	L4
	b)	Explain different switch logic used for designing of VLSI circuits.	8M	3	L2
		UNIT–IV			
7.	a)	With a neat diagram, explain 4-bit barrel shifter.	7M	4	L3
	b)	Explain architecture Field Programmable Gate Arrays with benefits.	7M	4	L2
		OR			
8.	a)	Write short note on Complex Programmable Logic Devices	7M	4	L2
	b)	Design an array multiplier and discuss the merits and demerits with an example.	7M	4	L3
		UNIT–V			
9.	a)	Compare the chip level test techniques, system-level test techniques	10M	5	L2
	b)	Describe stuck at ‘0’ and stuck at ‘1’ fault models with examples.	4M	5	L1
		OR			
10.	a)	Explain the concept of design verification and design capture tools used in VHDL synthesis.	10M	5	L1
	b)	Explain Need for testing,	4M	5	L1

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Code: 5G364

III B.Tech. II Semester Supplementary Examinations February 2021

Digital Signal Processing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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			Marks	CO	Blooms Level
		UNIT–I			
1.	a)	Test whether the following systems are linear, time-invariant, causal and stable or not i) $y(n) = x^3(n)$ ii) $y(n) = xe^{\|x(n-2)\|}$	8M		
	b)	Explain how linear convolution can be obtained using DFT and IDFT with an example.	6M		
		OR			
2.	a)	If x(n) denotes a finite length sequence of length N, show that $x((-n))_N = x((N-n))_N$.	6M		
	b)	Determine the frequency response of LTI system governed by the difference equation y(n) = x(n)+0.81x(n-1)+ 0.81x(n-2)-0.45y(n-2) using DFT.	8M		
		UNIT–II			
3.	a)	An 8 point sequence is given by x(n) = { 2,2,2,2,1,1,1,1 }. Compute the 8 point DFT of x(n) by radix – 2 D I T F F T.	8M		
	b)	Compute the IDFT of the following sequence using DIF algorithm X(K) = {5,0,1-j,0,1,0,1+j,0}	6M		
		OR			
4.	a)	Compare DIT FFT and DIF FFT algorithms.	7M		
	b)	Give the steps involved in implementing Radix –3, DIT FFT algorithm.	7M		
		UNIT–III			
5.	a)	Design a Chebyshev IIR LPF using Bilinear Transformation for T=1sec to satisfy th following specifications: $0.87 \le \left\|H(e^{j\mu})\right\| \le 1.0, \quad 0 \le \mu \le 0.25®$ $\left\|H(e^{j\mu})\right\| \le 0.35, \quad 0.375® \le \mu \le ®$	8M		
	b)	Determine the poles of low pass Butterworth filter for N=4. Sketch the location of pol on s-plane and hence determine the normalized transfer function of LPF.	6M		
		OR			
6.	a)	Using a rectangular window technique design a lowpass filter with passband gain of unity, cutoff frequency of 1000Hz and working at a sampling frequency of 5 kHz. The length of the impulse response should be 7.	8M		
	b)	Explain the principle of designing FIR filters using frequency sampling technique.	6M		
		UNIT–IV			
7.	a)	Explain the decimation process in the frequency domain.	7M		
	b)	Consider a ramp sequence and sketch its interpolated and decimated versions with a factor '3'.	7M		
		OR			
8.	a)	Plot the signals and their corresponding spectra for rational sampling rate conversion by (a) I / D =5 / 3 and (b)) I / D =3 / 5. Assume that the spectrum of the input signal x(n) occupies the entire range $-\pi \le w_x \le \pi$.	8M		
	b)	Mention the applications of Multirate DSP.	6M		
		UNIT–V			
9.	a)	Mention the applications of DSP.	7M		
	b)	Discuss about Spectral analysis of non-stationary signals.	7M		
		OR			
10.	a)	Briefly explain about signal compression techniques.	7M		
	b)	Discuss about oversampling A/D converter in signal processing.	7M		

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Code: 5G363

III B.Tech. II Semester Supplementary Examinations February 2021

Microprocessors & Interfacing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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			Marks	CO	Blooms Level
		UNIT–I			
1.	a)	Define Addressing Modes. Write down the examples for different types of 8086 addressing modes.	8M	1	L1
	b)	Classify Instruction Sets of 8086 Microprocessor.	6M	1	L2
		OR			
2.	a)	The physical branch address is 5A230 H when CS = 5200 H. Find the physical address if CS is changed to 7800 H.	7M	1	L6
	b)	Discuss the concept of Memory Addressing in 8086 with some example.	7M	1	L6
		UNIT–II			
3.	a)	Draw the pin diagram of 8086 microprocessors and explain the function of various pins in brief.	8M	2	L2
	b)	Explain structure of DRAM and SRAM Cells	6M	2	L2
		OR			
4.	a)	Distinguish between Minimum and Maximum Modes of 8086.	7M	2	L4
	b)	Discuss Memory Interfacing with 8086 Microprocessor.	7M	2	L6
		UNIT–III			
5.	a)	What are the functions to be performed by microprocessor while interfacing an ADC? Categorize ADC also.	7M	3	L4
	b)	Draw a PIN diagram of 8255 in brief.	7M	3	L3
		OR			
6.	a)	What are the different operating modes of of 8279?	7M	3	L1
	b)	Explain the operation of 8255 PPI Port A programmed as input and output in Mode 1 with necessary handshaking signals.	7M	3	L5
		UNIT–IV			
7.	a)	With functional block diagram, explain the operation and programming of 8251 in detail.	8M	4	L2
	b)	Show architecture of 8253 device with its silent features.	6M	4	L2
		OR			
8.	a)	What is RS-232C device and discuss its application with TTL.	7M	4	L6
	b)	Write a sample program of serial data transfer example with proper justification.	7M	4	L5
		UNIT–V			
9.	a)	Explain the flag register format of 80286 and 80386 with a suitable figure?	8M	5	L2
	b)	What is virtual memory? Explain with their advantage and disadvantage?	6M	5	L1
		OR			
10.	a)	With the neat diagram explain the interfacing of 80287 with 80286 microprocessor.	7M	5	L5
	b)	List the salient features of Pentium pro processors.	7M	5	L1

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