Code: 7G16D

R-17

III B.Tech. II Semester Supplementary Examinations May/June 2024
Object Oriented Programming Concepts
(Common to EEE & ECE)

Max. Marks: 70   Time: 3 Hours
Answer *any five full questions* by choosing one question from each unit (5x14 = 70 Marks)
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UNIT–I

1. a) Write short note on destructor. Explain with suitable example.   7M
    b) Explain merits and demerits of Object Oriented methodology.   7M

OR

2. a) Compare Object based programming and Object Oriented Programming. Explain how data and functions are organized in OOP.   7M
    b) Write the differences between pointers and arrays.   7M

UNIT–II

3. a) When do you use virtual base class? Explain with suitable example.   6M
    b) Explain function overloading and operator overloading with examples.   8M

OR

4. a) Explain operator overloading with the implementation of complex numbers.   7M
    b) Illustrate runtime polymorphism using virtual functions.   7M

UNIT–III

5. Explain the following string handlings with suitable example.
    i. String length   ii. Character Extraction iii. String comparison   14M

OR

6. a) How to assign the values to the variables in the class during the time of creation of an object to that class? Explain with an example.   7M
    b) Write a java program for checking Armstrong number.   7M

UNIT–IV

7. a) Write an example program to create threads using Thread class.   7M
    b) Write a program to explain the process of accessing interface variables.   7M

OR

8. a) What is multithreading and what are the advantages of multithreading?   7M
    b) Explain Creating Packages and Accessing a Package with examples.   7M

UNIT–V

9. a) List the types of byte & character streams in java. Explain any two byte streams & two character streams with a suitable example.   8M
    b) Write a simple applet program to display a string "I LIKE IPL MATCHES".   6M

OR

10. a) Discuss the Life Cycle of a Thread using a state transition diagram.   7M
    b) Demonstrate the creation of an applet using an example program   7M

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III B.Tech. II Semester Supplementary Examinations May / June 2024

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70   Time: 3 Hours

Answer *any five full questions* by choosing one question from each unit (5x14 = 70 Marks)

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UNIT–I

1. a) Explain CMOS fabrication using N-well process with neat diagrams. **8M**

    b) Explain about lithography process to pattern the oxide layer. **6M**

OR

2. a) Determine the Pull-up to Pull-down ratio for an nMOS inverter driven by another nMOS inverter? **8M**

    b) Draw the Bi-CMOS inverter with no static current flow and give its advantages. **6M**

UNIT–II

3. a) What are the alternative forms of pull ups in nMOS inverter? Write the advantages and disadvantages of each one. **8M**

    b) What scaling? Explain the limitations of scaling? **6M**

OR

4. a) Draw the circuit and stick diagram for AOI gate? **7M**

    b) Draw the Layout for AOI gate? **7M**

UNIT–III

5. Explain with suitable examples how to design the layout of a gate to maximize performance and minimize area **14M**

OR

6. Explain different wiring capacitances used in Gate level design with example **14M**

UNIT–IV

7. With the help of a block diagram explain the principle and operation of standard cells. **14M**

OR

8. Compare PLAs, PALs, CPLDs, FPGAs, and standard cells in all respects **14M**

UNIT–V

9. a) Explain test principles of VLSI circuits. **7M**

    b) Explain Programmable Logic Array(PLA) with an example **7M**

OR

10. a) What are the objectives of BIST? **7M**

    b) What is the need of testability? Explain design for testability **7M**

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Code: 7G364

III B.Tech. II Semester Supplementary Examinations May/June 2024

Digital Signal Processing

(Electronics and Communication Engineering)

Max. Marks: 70   Time: 3 Hours

Answer *any five full questions* by choosing one question from each unit (5x14 = 70 Marks)

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UNIT–I

1. a) Determine the particular solution of the difference equation
    y (n) = 5/6 y (n-1)-1/6 y (n-2) + x (n) when the forcing function is
    $x(n) = 2^n u (n)$ 7M
    b) Compute the convolution of $x(n)$ = u (n) – u (n – 5), $h (n)$ = [1, 2, 2, 1]   7M

OR

2. a) How are discrete time signals classified? Differentiate between them.   7M
    b) Discuss the concept of stability and causality with examples.   7M

UNIT–II

3. a) Compute 8-point DFT of a sequence x (n) ={1,-1,2,-1,3,0,4,-1} using DIT algorithm   10M
    b) Write the steps involved in computing FFT for composite N   4M

OR

4. a) Write the steps involved in DIF algorithm   7M
    b) Derive DIF - FFT algorithm for 8 point sequence and draw the butterfly diagram   7M

UNIT–III

5. a) Obtain the analog Chebyshev filter transfer function that satisfies the constraints
    1/ 2   H(j)   1; 0   2   H(j) <0.1 ;   4   9M
    b) Write about the salient features of IIR Structures Direct form–I, Direct form- II   5M

OR

6. Using a rectangular window technique, design a low pass filter with pass band gain of
    unity, cut-off frequency of 1000Hz and working at a sampling frequency of 5 KHz. The
    length of the impulse response should be 7.   14M

UNIT–IV

7. a) Explain about the need for Multirate Digital Signal Processing?   7M
    b) Consider a ramp sequence and sketch its interpolated and decimated versions with a
    factor '3'.   7M

OR

8. a) Obtain the necessary expression for interpolation process.   7M
    b) Discuss the applications of multi-rate signal processing.   7M

UNIT–V

9. a) Explain the major blocks in Musical sound processing.   7M
    b) Discuss spectral analysis of non stationary signals in DSP.   7M

OR

10. Compare and contrast
    i.   Stationary Vs. nonstationary signals
    ii. Oversampling A/D Converter Vs. Oversampling D/A Converter   14M

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