Hall Ticket Number :										

R-17

Code: 7G16D

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2023

Object Oriented Programming Concepts

(Common to EEE & ECE)

Max. Marks: 70 Time: 3 Hours

Answer *any five full questions* by choosing one question from each unit (5x14 = 70 Marks)

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UNIT–I

1.	a)	Write short note on destructor. Explain with suitable example.	7M
	b)	Explain merits and demerits of Object Oriented methodology.	7M
		OR	
2.	a)	Define structure. Explain with any suitable example program.	8M
	b)	List and explain data types in C++.	6M

UNIT–II

3.	a)	When do you use virtual base class? Explain with suitable example.	6M
	b)	Explain function overloading and operator overloading with examples.	8M
		OR	
4.	a)	Define Inheritance. Write a C++ program to demonstrate multiple inheritances.	7M
	b)	What is mean by Overloading? Explain about function overloading with suitable program.	7M

UNIT–III

5.	a)	What is an array? Discuss various array definitions in java with an example.	7M
	b)	Discuss about primitive data types.	7M
		OR	
6.	a)	Define Class & Object in Java? Explain with suitable example.	7M
	b)	Write a java program to print first N Fibonacci Series using While loop.	7M

UNIT–IV

7.	a)	How to define a user exception in a program? Illustrate with an example.	7M
	b)	Write the steps involved in adding a class to a package.	7M
		OR	
8.	a)	What is a Thread? How are threads created?	7M
	b)	Write an example program to create threads using Thread class.	7M

UNIT–V

9.	a)	List the types of character streams in java. Explain any four character streams with a suitable example.	8M
	b)	Demonstrate the passing parameters to the applet with example.	6M
		OR	
10.	a)	What is an Applet? Explain how to create an Applet.	7M
	b)	What is multithreading? What are the priorities given for multithreading.	7M

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Hall Ticket Number :										

R-17

Code: 7G361

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2023

VLSI Design

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *any five full questions* by choosing one question from each unit (5x14 = 70 Marks)

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UNIT–I

1. a) Explain the fabrication of Bi-CMOS technology with relevant diagrams. 9M
   b) Draw the transfer characteristics of CMOS inverter and explain. 5M

OR

2. a) Derive the relationship between pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter(Zpu/Zpd) 9M
   b) List the differences between CMOS and Bipolar technologies. 5M

UNIT–II

3. a) Explain CMOS design rules for wires, contacts and transistors layout diagrams for CMOS inverters. 7M
   b) Explain the layers NMOS. 7M

OR

4. a) Prepare the stick diagram and layout diagram for NAND gate using CMOS encoding style. 7M
   b) Discuss in detail about scaling and derive scaling factors for various parameters 7M

UNIT–III

5. Derive an expression for sheet resistance (Rs) and apply the concept for calculation of sheet resistance for CMOS inverter. 14M

OR

6. a) Draw the circuit diagram of inverting type NMOS Super buffer and explain. 6M
   b) Calculate inverter resistance for nMOS with Zpu=4 for pull up transistor and Zpd=1for pull down transistor and for CMOS Zpu=1 for pull up transistor and Zpd=1 for pull down transistor. 8M

UNIT–IV

7. a) With a neat diagram, explain 4-bit barrel shifter. 7M
   b) Design an array multiplier and discuss the merits and demerits with an example. 7M

OR

8. a) Explain 4-bit Serial- parallel multiplier with a neat diagram. 7M
   b) Explain about High density memory elements with neat diagrams. 7M

UNIT–V

9. a) What is testing? Discuss the importance of testing? 6M
   b) Explain about chip level test techniques? 8M

OR

10. a) What are the test principles to test the circuit? 6M
    b) Discuss about design capture tools and design verification tools? 8M

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Hall Ticket Number :										

R-17

Code: 7G364

III B.Tech. II Semester Supplementary Examinations Nov/Dec 2023

Digital Signal Processing

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

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Answer *five* questions by choosing one question from each unit (5 x 14 = 70 Marks)

			Marks	CO	BL
		UNIT–I			
1.	a)	Check the following system described with difference equations for linearity, shift invariance, memory and causality; $y[n] - y[n-1] = x[n]$.	7M	CO1	L2
	b)	Determine the impulse response for the cascade of two LTI systems having impulse responses $h_1[n] = \left(\frac{1}{2}\right)^n u[n]$ and $h_2[n] - \left(\frac{1}{4}\right)^n u[n]$.	7M	CO1	L3
		OR			
2.	a)	Define DFT and IDFT. State any Four properties of DFT.	7M	CO1	L2
	b)	Find the IDFT of the sequence X(K) = {2, 2-3j, 4, 2+3j}.	7M	CO1	L2
		UNIT–II			
3.		Compute the eight-point DFT of the sequence by using DIF FFT algorithm. $x(n) = \begin{cases} 1, & 0 \le n \le 7 \\ 0, & otherwise \end{cases}$	14M	CO1	L3
		OR			
4.		Draw the radix–2, 8–point DIT FFT flow graph obtained by the DFT sequence; x[n] = {1, 1,1,1,1,1,1,1}.	14M	CO1	L3
		UNIT–III			
5.	a)	Using Bilinear transformation, design a high pass filter, monotonic in pass band with cutoff frequency of 1000 Hz and down 10dB at 350 Hz. The sampling frequency is 5000 Hz.	7M	CO2	L2
	b)	Explain the procedure for designing Analog filters using the Chebyshev approximation.	7M	CO2	L2
		OR			
6.	a)	Design an FIR linear-phase, digital filter approximating the ideal frequency response Hd (ω) = 1 for $\|\omega\| \le \pi/6$; 0 for $\pi/6 < \|\omega\| \le \pi$, using a Hamming window.	7M	CO2	L3

	b)	Design a FIR digital low-pass filter with a cutoff frequency of 1 kHz and a sampling rate of 4 kHz with 7 samples using Fourier series method	7M	CO2	L3

UNIT–IV

7.		Explain about sampling rate conversion by a rational factor I/D.	14M	CO3	L2

OR

8.		Discuss about multistage implementation of sampling rate conversion.	14M	CO3	L2

UNIT–V

9.		Explain about Spectral analysis of non-stationary Signals.	14M	CO4	L2

OR

10.	a)	Explain sub-band coding of speech signals in detail.	7M	CO4	L2
	b)	Explain over sampling A/D and D/A conversion.	7M	CO4	L2

*** End ***