Hall Ticket Number :

Code : 1G371

R-11

IV B.Tech. I Semester Regular & Supplementary Examinations Nov/Dec 2015

Optical Communications

(Electronics & Communication Engineering)

Max. Marks: 70 Time: 03 Hours

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1. a) Discuss the Historical Developments of Optical Fiber Communications
   b) Discuss advantages of optical fiber communications

2. a) Discuss in brief about Fiber Materials
   b) Given core refractive index of 1.48 and relative refractive index difference 1.5% for a single mode fiber operating at 0.85μm, Find i) the maximum core diameter ii) new maximum core diameter if relative refractive index difference is reduced by a factor of 10.

3. a) Write about Intrinsic absorption and Extrinsic absorption Losses in Silica Glass Fibers.
   b) Explain the concept of Dispersion in fiber losses in detail.

4. a) The total efficiency of an injection laser with a GaAs active region is 18%. The voltage applied to the device is 2.5 V and the band gap energy for GaAs is 1.43 eV. Calculate the external power efficiency of the device.
   b) Discuss about Laser diode Modes and its threshold conditions.

5. a) Discuss about Lensing Schemes for Coupling Improvement.
   b) Explain LED Coupling to single mode fibers.

6. a) Write about Avalanche Multiplication Noise
   b) Explain in brief about Noise concept in Photo detector.

7. Discuss basic elements in Analog links with block diagram.

8. a) Discuss about Fiber grating filters.
   b) Explain the operational principles of WDM.

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Hall Ticket Number :										

Code : 1G478 **R-11**

IV B.Tech. I Semester Regular & Supplementary Examinations Nov/Dec 2015

Computer Networks

(Electronics & Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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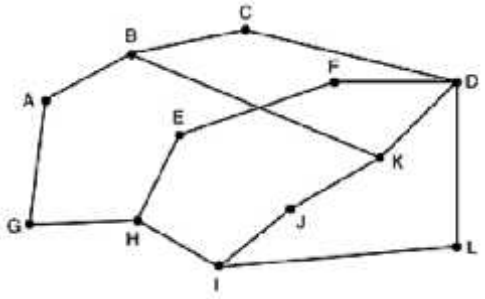
1. a) Elucidate the functionality of ADSL 7M
   b) Explain the protocol and layer functionality of TCP/IP model 7M
2. a) What is framing? Explain bit stuffing and byte stuffing in framing 8M
   b) A channel has a bit rate of 4 kbps and a propagation delay of 20 msec. For what range of frame sizes does stop-and-wait give an efficiency of at least 50 percent? 6M
3. a) What is collision free protocol? 2M
   Describe the following contention free protocols
   i. bitmap protocol 3M
   ii. binary countdown protocol 3M
   b) Consider building a CSMA/CD network running at 1 Gbps over a 1-km cable with no repeaters. The signal speed in the cable is 200,000 km/sec. What is the minimum frame size? 6M
4. a) Describe leaky bucket algorithm in wireless network routing 7M
   b) Compute a multicast spanning tree for router C in the following subnet for a group with members at routers A, B, C, D, E, F, I, and K.



7M

5. a) Differentiate the protocols of OSPF and BGP with suitable example 10M
   b) A network on the Internet has a subnet mask of 255.255.240.0. What is the maximum number of hosts it can handle? 4M
6. Explain the steps to establish and release TCP connection management using finite state transition diagram 14M
7. a) Write short notes on WWW with suitable diagram 8M
   b) Explain the following
   i. IMAP
   ii. Cookies
   iii. MIME 6M
8. a) What is DES? Explain the working procedure of DES 10M
   b) What is quantum cryptography? Give an example 4M

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Hall Ticket Number :										

Code : 1G373 **R-11**

IV B.Tech. I Semester Regular & Supplementary Examinations Nov/Dec 2015

Digital Design Through Verilog HDL

(Electronics & Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1.		Explain various levels of abstraction and major activities in ASIC design with neat diagrams?	14M
2.		Explain about various lexical tokens available in Verilog with suitable examples.	14M
3.		Write Verilog code for a typical AOI gate and also write the test bench program with neat diagrams, truth tables and simulation waveforms.	14M
4.	a)	Write Verilog code for two 4-bit adder using full adder and half adder with neat block diagrams	8M
	b)	Write Verilog code for D-Latch with neat block diagrams	6M
5.		Write Verilog code for CMOS Inverter and 2 – input CMOS NOR gate with neat circuit diagrams and also write the test bench program for it.	14M
6.	a)	Explain Melay machine FSM with neat block diagram.	6M
	b)	Write Verilog code for Sequence generator using Melay machine FSM.	8M
7.	a)	Explain about FPGA with neat block diagrams	7M
	b)	Explain about CPLD with neat block diagrams	7M
8.	a)	Design UART using Verilog HDL	8M
	b)	Write about 486 Bus model	6M

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Hall Ticket Number :										

Code : 1G372 **R-11**

IV B.Tech. I Semester Regular & Supplementary Examinations Nov/Dec 2015

Digital Signal Processing

(Common to EEE & ECE)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1. a) Test the stability of LTI systems, whose impulse responses are,

i). $h(n) = (0.2)^n u(n)$. ii). $h(n) = (0.3)^n u(n) + 2^n u(n)$. 8M

b) A causal system is represented by the following difference equation

$y(n) + \frac{1}{4} y(n-1) = x(n) + \frac{1}{2} x(n-1)$. Find the system transfer function H(z) and the impulse response. 6M

2. Let x(n) be a real sequence of length – N and its N - point DFT is given by X(K), Show that:

a. X(N-K) = X^*(k)

b. X(0) is real,

c. If N is even, then X(N/2) is real. 14M

3. a) Find the 8–point DFT of real sequence x(n)={1,2,2,2,1,0,0,0} by using DIF-FFT algorithm. 7M

b) Show that the direct computation of the *N*-point DFT of a length-*N* sequence requires $4N^2$ real multiplications and (4*N*-2) N real additions. 7M

4. a) A linear time invariant system is described by the following input-output relation 2y(n)-y(n-2)-4y(n-3) = 3x(n-2).Realize the system in the following form:

i) Direct form-I realization.

ii) Transposed realization of Direct form-II. 7M

b) Realize the given system function $H(z) = 1 + \frac{1}{4} z^{-1} + \frac{17}{8} z^{-2} + \frac{1}{4} z^{-3} + z^{-4}$ by using :

i. Direct form

ii. The linear phase form. 7M

5. Determine the system function H(z) of the lowest order Chebyshev filter that meet the following specifications:

a. 3dB ripple in the pass band $0 \le |w| \le 0.3®$

b. At least 20 dB attenuation in the stop band $0.6® \le |w| \le ®$.

Use the Bilinear transformation. 14M

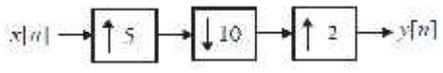
6. A low pass filter is to be designed with the following desired frequency response

$H_d(e^{jw}) = H_d(w) = \begin{cases} e^{-j2w}, & |w| < \frac{®}{4} \\ 0, & \frac{®}{4} < |w| < ® \end{cases}$. Determine the filter coefficients $h_d(n)$ and h(n) if w(n) is rectangular window defined as follows: $w_R(n) = \begin{cases} 1, 0 \le n \le 4 \\ 0, otherwise \end{cases}$.

Also, find the frequency response, H(w) of resulting FIR filter. 14M

7. a) Show that the up-sampler and down sampler are the time invariant systems. 7M

b) Develop an expression for the output y[n] as a function of the input x[n] for the multirate structure of given figure.



7M

8 Explain about Discrete Multitone Transmission of digital data. 14M

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Hall Ticket Number :										

Code : 1G374 **R-11**

IV B.Tech. I Semester Regular & Supplementary Examinations Nov/Dec 2015

Embedded Systems

(Electronics & Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1. a) What is an embedded system? Write a brief note on different development tools available for embedded systems. 7M
   b) Write a brief note on recent trends and memory of embedded systems. 7M

2. a) What are the major components of the embedded system hardware? Explain briefly. 7M
   b) What are the services provided by an operating system? Explain. 7M

3. Explain the following with detailed examples 5M
   a) Data Transfer Instructions 5M
   b) Arithmetic Instructions 4M
   c) Logical Instructions

4. a) Write an assembly language program to generate a square wave of 1 KHz at port pin 1.5 using auto reload mode of timer 0 7M
   b) Explain timer flag interrupt, serial port interrupt and external interrupts with example. 7M

5. Explain the process of interfacing a 4X4 Hexadecimal keyboard to 8051 with a clear interface diagram and program 14M

6. a) Explain serial communication using I^2C and CAN protocols. 7M
   b) Explain in detail IEEE 802.11 7M

7. Compare semaphores, events and queues for implanting inter task communication with an example 14M

8. a) Explain in detail the basic functions in developing a RTOS. 7M
   b) Explain memory management system of multitasking RTOS. 7M

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Hall Ticket Number :										

Code : 1G376 **R-11**

IV B.Tech. I Semester Regular & Supplementary Examinations Nov/Dec 2015

Radar Engineering

(Electronics & Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1. a) Draw the block diagram of the basic radar system and explain the operation of each block in detail. 7M

   b) A Radar transmitter has a peak pulse power of 250 KW, apRF of1200 pps. If the pulse width is 0.8 sec. Calculate
      i. Maximum unambiguous range.
      ii. The duty cycle.
      iii. Avg. it transmitter power and
      iv. A suitable bandwidth. 7M

2. a) What are components of an elementary form of Radar? Explain how it works? 7M

   b) Derive the simple form of radar equation. 7M

3. a) What is Doppler frequency shift? Establish a relation between Doppler frequency shift and radial velocity of a moving target. 7M

   b) Explain how isolation between transmitter & receiver of a radar system can be achieved? 7M

4. a) With neat sketch explain FMCW radar. Obtain the beat frequency for different modulation techniques. 9M

   b) Write a short note on system losses 5M

5. a) Explain the limitations of MTI radar in detail. 7M

   b) Compare MTI and pulse Doppler radar. 7M

6. a) Discuss the effect of surface quality and reflection characteristics of a target on the angular tracking accuracy of a tracking radar. 7M

   b) Describe the phase comparison mono pulse tracking technique in a radar system with the help of necessary block diagram. 7M

7. a) Derive the impulse response of a matched filter that is commonly used in a radar receiver. 7M

   b) Define noise figure and equivalent noise temperature of a radar receiver. 7M

8. a) List out the different types of displays used for radar applications, and their characteristics. 7M

   b) What are the advantages, limitations, and applications of antenna arrays in radar systems? 7M

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