

Code: 19A373T

IV B.Tech. I Semester Regular Examinations Nov/Dec 2022

Management science

(Common to ECE & CSE)

Max. Marks: 70

Time: 3 Hours

Answer any five full questions by choosing one question from each unit (5x14 = 70 Marks)

Marks CO BL

UNIT-I

1. What do you mean by management? Explain in detail the principles of management under the Henri Fayol's administration

14M 1 2

OR

2. Explain the principles and types of organizational structures.

14M 1 2

UNIT-II

3. Define EOQ? What are the factors that determine EOQ?

14M 2 2

OR

4. a) What are types of channels of Distribution?
b) What is market mix? Explain

7M 2 2

7M 2 2

UNIT-III

5. What do you understand about performance appraisal? Discuss the various tool and techniques of performance appraisal

14M 3

OR

6. Briefly explain the process of recruitment and selection process

14M 3

UNIT-IV

7. An R&D projects has a list of tasks to be performed whose time estimates are given in the table

Activity (i-j)	Activity name	t _o	t _m	t _p
1-2	A	4	6	8
1-3	B	2	3	10
1-4	C	6	8	16
2-4	D	1	2	3
3-4	E	6	7	8

Activity (i-j)	Activity name	t _o	t _m	t _p
3-5	F	6	7	14
4-6	G	3	5	7
4-7	H	4	11	12
5-7	I	2	4	6
6-7	J	2	9	10

- a. Draw the project network b. find the critical path
c. Find the probability that the project is completed in 19 days. if the probability is less 20%, find the probability of completing it in 24 days

14M 4 3

OR

8. a) What are the functions of working capital?
b) State the cost of capital.

7M 4 2

7M 4 2

UNIT-V

9. a) Write short notes on Total Quality Management (TQM)
b) Define business ethics. Write the importance of ethics in organization

7M 5 2

7M 5 2

OR

10. a) What is Management Information System (MIS)?
b) State the needs for Supply Chain Management and its potential benefits.

7M 5 2

7M 5 1

END

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IV B.Tech. I Semester Regular Examinations Nov/Dec 2022

Non-Conventional Sources of Energy

(Common to ME & ECE)

Max. Marks: 70

Time: 3 Hours

Answer any five full questions by choosing one question from each unit (5x14 = 70 Marks)

	Marks	CO	BL
UNIT-I			
1. a) Explain the following terms related to Solar radiation Geometry: i) Altitude Angle ii) Declination Angle iii) Solar Azimuth angle	6M	CO1	L2
b) Explain the working of any one type of instrument used for the measurement of Global solar radiation.	8M	CO1	L2
OR			
2. a) What are the advantages and limitations of renewable energy sources?	4M	CO1	L1
b) Derive an expression for total radiation on inclined surface.	10M	CO1	L3
UNIT-II			
3. a) Enumerate and explain in brief the different types of concentrating type collectors.	7M	CO2	L2
b) Explain in detail about the passive Solar Space heating System.	7M	CO2	L2
OR			
4. a) Explain the main components of a flat plate Solar collector with a neat diagram.	7M	CO2	L2
b) With the aid of a neat sketch, explain the working of a Solar pond.	7M	CO2	L2
UNIT-III			
5. a) Discuss the various factors that affect the production of biogas.	7M	CO3	L2
b) Explain the constructional features of any one type of bio-gas plant.	7M	CO3	L2
OR			
6. a) Describe the main considerations in selecting a site for wind generators.	6M	CO3	L2
b) Derive an expression for the maximum wind power that can be extracted using Betz criteria?	8M	CO3	L6
UNIT-IV			
7. a) What are the merits and demerits of geothermal energy?	7M	CO4	L1
b) Explain the operation of an oscillating water type of wave device.	7M	CO4	L2
OR			
8. a) Explain in detail about the Liquid dominated geothermal system.	7M	CO4	L2
b) Explain the working of an Ocean thermal energy conversion plant (OTEC) with a neat diagram.	7M	CO4	L2
UNIT-V			
9. a) Explain liquid metal system of MHD power generation with a neat schematic.	8M	CO5	L2
b) Write short notes on the following: (i) Criterion for selection of material for thermo electric generators (ii) Carnot cycle	6M	CO5	L2
OR			
10. a) Explain Peltier and Joule effects.	4M	CO5	L2
b) With the aid of a neat sketch explain the working of a thermoelectric power generator.	10M	CO5	L2

END

Code: 19A47CT

IV B.Tech. I Semester Regular Examinations Nov/Dec 2022

Wireless Communication & Networks

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

Answer any five full questions by choosing one question from each unit (5x14 = 70 Marks)

Marks CO BL

UNIT-I

1. Describe the working mechanism for various types of Carrier Sense Multiple Access (CSMA) protocols.

14M 1 L1

OR

2. Describe the popularly known Multiple Access Techniques with suitable examples.

14M 1 L1

UNIT-II

3. Explain the following in detail :

SS7 Probe, SS7 Vulnerability and SS7 Protocol suite

14M 2 L2

OR

4. Explain the following in detail :

B-ISDN architecture, B-ISDN interactive services and B-ISDN distribution services

14M 2 L2

UNIT-III

5. Illustrate the WAP protocol stack with suitable diagram.

14M 3 L3

OR

6. Illustrate the following in detail with suitable diagrams :

- a) Mobile node residing on home network
b) Mobile node moving to a foreign network
c) Mobile IP with reverse tunneling

14M 3 L3

UNIT-IV

7. Outline spread spectrum, narrowband microwave and infrared transmission techniques for the attributes :

Frequency, Maximum coverage, transmit power, rated speed (% of 10 mbps)

14M 4 L4

OR

8. Illustrate the working mechanism of Bluetooth communications. Highlight specifications given by Bluetooth Core Specification Working Group (CSWG).

14M 4 L4

UNIT-V

9. Summarize the technical specifications and operational capabilities of GPRS.

14M 5 L5

OR

10. Summarize the technical specifications and operational capabilities of GSM.

14M 5 L5

END

Code: 19A47DT

IV B.Tech. I Semester Regular Examinations Nov/Dec 2022

Digital IC Design

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

Answer any five full questions by choosing one question from each unit (5x14 = 70 Marks)

		Marks	CO	BL
UNIT-I				
1. a)	What is Switching Threshold? Derive Switching Threshold expression of Static CMOS inverter.	7M	1	L4
b)	Draw and explain the overall shape of the Voltage-Transfer characteristics of the static CMOS inverter.	7M	1	L3
OR				
2. a)	Illustrate the Switch models of CMOS inverter. Also, list and explain the important properties of Static CMOS related to this switch level view.	8M	1	L2
b)	Discuss about propagation delay.	6M	1	L2
UNIT-II				
3. a)	Discuss the basic concept of Complementary pass-transistor logic (CPL). Draw and explain schematic of four-input NAND-gate using CPL.	8M	2	L2
b)	Why domino gate input values must be monotonically increased? Elaborate.	6M	2	L3
OR				
4. a)	Explain the following approaches used to reduce delays in large fan-in circuits: i) Transistor sizing ii) Progressive Transistor sizing iii) Input Re-Ordering iv) Logic Restructuring	8M	2	L2
b)	Design a Domino 3-input OR gate and then explain its operation.	6M	2	L2
UNIT-III				
5.	Compute the logical effort of transistor sizing	14M	3	L4
OR				
6.	Explain about power consumption in CMOS gates	14M	3	L2
UNIT-IV				
7.	Discuss the following w.r.t based design rules: i. Design rules for wires ii. Transistor (nMOS, pMOS and CMOS) design rules	14M	4	L4
OR				
8. a)	Describe how large capacitive loads are driven.	7M	4	L3
b)	What is the need for design rules? What happens if design rules are not followed? Elaborate.	7M	4	L2
UNIT-V				
9. a)	Draw the circuit topology of the CMOS SRAM cell and then with the help of equivalent circuits, explain its read and write operation.	7M	5	L3
b)	Explain about modified Booth's Multiplier.	7M	5	L2
OR				
10. a)	Draw and explain 2 input NAND circuit and then develop its stick diagram.	7M	5	L2
b)	Explain the operation of a 4 x 4 Barrel shifter circuit.	7M	5	L2

END

Code: 19A471T

IV B.Tech. I Semester Regular Examinations Nov/Dec 2022

Embedded Systems

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

Answer any five full questions by choosing one question from each unit (5x14 = 70 Marks)

Marks CO BL

UNIT-I

- | | | | |
|---|----|---|---|
| 1. a) Discuss various addressing modes of 8051 microcontroller with examples. | 7M | 1 | 2 |
| b) Explain pin configuration of 8051 with diagram. | 7M | 1 | 2 |

OR

- | | | | |
|--|-----|---|---|
| 2. a) Design and develop a program for interfacing of stepper motor with 8051 microcontroller to rotate stepper motor in clockwise direction continuously in full step mode. | 10M | 1 | 5 |
| b) Describe the interfacing diagram of DAC to 8051. | 4M | 1 | 2 |

UNIT-II

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|---|-----|---|---|
| 3. Summarize the major key application areas of embedded systems with appropriate real-time examples. | 14M | 2 | 4 |
|---|-----|---|---|

OR

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|--|----|---|---|
| 4. a) Evaluate the key steps involve in embedded system architecture by considering any example. | 5M | 2 | 5 |
| b) Explain about significance and classification of embedded system in detail. | 9M | 2 | 2 |

UNIT-III

- | | | | |
|---|----|---|---|
| 5. a) Explain about importance of Real Time Clock (RTC) and Watchdog timer in embedded system architecture. | 7M | 3 | 2 |
| b) Describe the working process of embedded operating system in detail. | 7M | 3 | 4 |

OR

- | | | | |
|--|-----|---|---|
| 6. Explain the hardware architecture of an embedded systems. | 14M | 2 | 2 |
|--|-----|---|---|

UNIT-IV

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|--|----|---|---|
| 7. a) Explain about the I2C protocol with neat sketch. | 7M | 4 | 2 |
| b) Illustrate the working function of USB and Bluetooth external communication protocols and how they interface to any microcontroller during embedded product design. | 7M | 4 | 2 |

OR

- | | | | | |
|-------|--|----|---|---|
| 8. a) | Explain about RS-232 serial interface in detail. | 7M | 4 | 2 |
| b) | Briefly explain how data transaction is carried out using CAN Bus with neat sketches also draw the CAN data frame and explain. | 7M | 4 | 4 |

UNIT-V

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|----|--|-----|---|---|
| 9. | Discuss the kernel objects of real time operating systems. | 14M | 5 | 2 |
|----|--|-----|---|---|

OR

- | | | | | |
|--------|---|----|---|---|
| 10. a) | What is priority inversion? What are the different techniques adopted for handling priority inversion? | 7M | 5 | 2 |
| b) | What is inter process communication (IPC)? Give an overview of different IPC mechanisms adopted by various operating systems? | 7M | 5 | 2 |

*****END*****

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IV B.Tech. I Semester Regular Examinations Nov/Dec 2022

FPGA Architectures and Applications

(Electronics and Communication Engineering)

Max. Marks: 70

Time: 3 Hours

Answer any five full questions by choosing one question from each unit (5x14 = 70 Marks)

Marks CO BL

UNIT-I

- | | | | | |
|-------|---|----|---|---|
| 1. a) | Explain different types of simple programmable logic devices | 7M | 1 | 2 |
| b) | Implement the functions $F1 = A'BC + AB'C + ABC$ $F2 = A'B'C' + A'B'C + ABC$ using PLA. | 7M | 3 | 6 |

OR

- | | | | | |
|-------|--|----|---|---|
| 2. a) | Explain ALTERA flex 10K series architecture. | 7M | 2 | 2 |
| b) | Show the structure of Cypress 370 series CPLD and explain. | 7M | 3 | 3 |

UNIT-II

- | | | | | |
|-------|--|-----|---|---|
| 3. a) | Show the structure of FPGA. | 4M | 1 | 3 |
| b) | Determine the steps in FPGA design flow. | 10M | 2 | 3 |

OR

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|-------|--|----|---|---|
| 4. a) | What is technology mapping .what is its importance | 7M | 2 | |
| b) | Explain LUT and multiplexer based mapping | 7M | 3 | 2 |

UNIT-III

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|-------|----------------------------------|-----|---|---|
| 5. a) | Explain the ALTERA Flex 8000 LAB | 10M | 2 | 2 |
| b) | Show the structure of Actel FPGA | 4M | 2 | 3 |

OR

- | | | | | |
|-------|---|-----|---|---|
| 6. a) | Explain Xilinx XC4000 CLB | 10M | 2 | 2 |
| b) | Show the structure of AT&T-ORCA's FPGA programmable functional unit | 4M | 2 | 3 |

UNIT-IV

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|-------|--|----|---|---|
| 7. a) | Draw and explain Mealy FSM and discuss the issues in designing | 7M | 1 | 2 |
| b) | What is state transition table and with example explain how it is formed from state diagram. | 7M | 1 | 2 |

OR

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|-------|---|-----|---|---|
| 8. a) | Illustrate basic concept of Petri nets for state machines | 10M | 1 | 3 |
| b) | Explain about One Hot State machine | 4M | 3 | 2 |

UNIT-V

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|----|---|-----|---|---|
| 9. | Explain one to three pulse generator using non registered PLD's | 14M | 3 | 2 |
|----|---|-----|---|---|

OR

- | | | | | |
|-----|--|-----|---|---|
| 10. | Explain about the data path and functional partition of FSM system level design? | 14M | 1 | 2 |
|-----|--|-----|---|---|

END