Hall Ticket Number :										

R-11 / R-13

Code: 1G478

IV B.Tech. I Semester Supplementary Examinations August 2020

Computer Networks

(Electronics & Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1.	a)	Elucidate the functionality of ADSL	7M
	b)	Explain the protocol and layer functionality of TCP/IP model	7M
2.	a)	Explain one bit sliding window protocol for normal and abnormal cases	8M
	b)	Hamming code is used for 16 bit message transmission. How many check bits are needed to ensure that the receiver can detect and correct single bit errors? Show the bit pattern transmitted in the message 1101001100110101.	6M
3.	a)	What is collision free protocol? Describe the following contention free protocols, i) bitmap protocol ii) binary countdown protocol	8M
	b)	Consider building a CSMA/CD network running at 1 Gbps over a 1-km cable with no repeaters. The signal speed in the cable is 200,000 km/sec. What is the minimum frame size?	6M
4.	a)	What is flooding? Describe Bellman-Ford routing algorithm with suitable network scenario example and routing table.	10M
	b)	List the two major differences between the warning bit method and the RED method	4M
5.	a)	Distinguish RARP, BOOTP, and DHCP with respect to the internetwork	7M
	b)	What is three bears problem? Explain the basic concept of CIDR	7M
6.		Explain the steps to establish and release TCP connection management using finite state transition diagram	14M
7.	a)	What is the significance of the Domain Naming System? Write a short note on DNS Name Space	7M
	b)	How does the user get the emails from the ISP's message transfer agent?	7M
8.	a)	What is DES? Explain the working procedure of DES	7M
	b)	What is quantum cryptography? Give an example	7M

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Hall Ticket Number :										

R-11 / R-13

Code: 1G373

IV B.Tech. I Semester Supplementary Examinations August 2020

Digital Design Through Verilog HDL

(Electronics & Communication Engineering)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1.		Explain various levels of abstraction and major activities in ASIC design with neat diagrams?	14M
2.		Explain about various lexical tokens available in Verilog with suitable examples.	14M
3.		Write Verilog code for a typical AOI gate and also write the test bench program with neat diagrams, truth tables and simulation waveforms.	14M
4.	a)	Write Verilog code for 4bit by 4bit multiplier with neat block diagrams	9M
	b)	Write various delays available in Verilog?	5M
5.		Write Verilog code for CMOS Inverter and 2 – input CMOS NOR gate with neat circuit diagrams and also write the test bench program for it.	14M
6.	a)	Explain Moore machine FSM with neat block diagram.	6M
	b)	Write Verilog code for Sequence generator using Moore machine FSM.	8M
7.	a)	Explain about FPGA with neat block diagrams	7M
	b)	Explain about CPLD with neat block diagrams	7M
8.	a)	Design UART using Verilog HDL	8M
	b)	Write about Static RAM.	6M

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Hall Ticket Number :										

R-11 / R-13

Code: 1G372

IV B.Tech. I Semester Supplementary Examinations August 2020

Digital Signal Processing

(Common to EEE & ECE)

Max. Marks: 70 **Time: 03 Hours**

Answer *any five* questions

All Questions carry equal marks (14 Marks each)

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1. a) Test the stability of LTI systems, whose impulse responses are,

i). $h(n) = (0.2)^n u(n)$. ii). $h(n) = (0.3)^n u(n) + 2^n u(n)$. 8M

b) A causal system is represented by the following difference equation $y(n) + \frac{1}{4} y(n-1) = x(n) + \frac{1}{2} x(n-1)$. Find the system transfer function H(z) and the impulse response. 6M

2. Let x(n) be a real sequence of length – N and its N - point DFT is given by X(K), Show that:

a. X(N-K) = X^*(k)

b. X(0) is real,

c. If N is even, then X(N/2) is real. 14M

3. a) Find the 8–point DFT of real sequence x(n)={1,1,1,1,0,0,0,0} by using DIF-FFT algorithm. 10M

b) What is in-place algorithm and what is the advantage of this algorithm? 4M

4. a) A linear time invariant system is described by the following input-output relation 2y(n)-y(n-2)-4y(n-3) = 3x(n-2).Realize the system in the following form:

i) Direct form-I realization.

ii) Transposed realization of Direct form-II. 7M

b) Realize the given system function $H(z) = 1 + \frac{1}{4} z^{-1} + \frac{17}{8} z^{-2} + \frac{1}{4} z^{-3} + z^{-4}$ by using :

i. Direct form

ii. The linear phase form. 7M

5. Given $H_a(s) = \frac{16(s+2)}{(s^2 + 2s + 5)(s+3)}$. Find H(z) using impulse invariant transformation. Assume T=0.2 sec. 14M

6. A low pass filter is to be designed with the following desired frequency response $H_d(e^{jw}) = H_d(w) = \begin{cases} e^{-j2w}, & |w| < \frac{®}{4} \\ 0, & \frac{®}{4} < |w| < ® \end{cases}$. Determine the filter coefficients $h_d(n)$ and h(n) if w(n) is rectangular window defined as follows: $w_R(n) = \begin{cases} 1, 0 \le n \le 4 \\ 0, otherwise \end{cases}$.

Also, find the frequency response, H(w) of resulting FIR filter. 14M

7. a) Show that the up-sampler and down-sampler satisfy the property of commutation if they are co-prime. 7M

b) Explain the ploy phase decomposition of an IIR filter with example. 7M

8 Explain about Discrete Multitone Transmission of digital data. 14M

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