Hall Ticket Number :										

R-15

Code: 5G472

IV B.Tech. I Semester Supplementary Examinations July 2021

Computer Networks

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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			Marks	CO	Blooms Level
		UNIT–I			
1.	a)	Illustrate each layer in OSI Model.	7M	1	3
	b)	Describe function of each layer in TCP/IP Model.	7M	1	2
		OR			
2.	a)	Demonstrate PSTN structure with explanation.	8M	1	3
	b)	Discuss role of protocols & their standards referred in data communication.	6M	1	2
		UNIT–II			
3.	a)	Demonstrate working of sliding window protocols.	7M	2	3
	b)	Describe CSMA/CD in detail.	7M	2	2
		OR			
4.	a)	Summarize Multiple Access Protocols.	7M	2	2
	b)	Explain various IEEE 802.X frame formats.	7M	2	2
		UNIT–III			
5.	a)	Compare adaptive and non-adaptive routing algorithms.	8M	3	5
	b)	Give Outline of an IP address? Discuss the class field in IP address.	6M	3	4
		OR			
6.	a)	Define fragmentation and explain why the IP4 and IP6 protocols need to fragment some packets.	7M	3	1
	b)	Examine role of Congestion Control Algorithms in communication.	7M	3	3
		UNIT–IV			
7.	a)	Show TCP and UDP Headers format with description.	8M	4	3
	b)	Draw the segment structure of TCP.	6M	4	4
		OR			
8.	a)	Justify the performance issues in transport layer protocols.	7M	4	5
	b)	Discuss application of Transport layer in data communication.	7M	4	2
		UNIT–V			
9.	a)	State advantages and limitations of public and secret key encryption.	6M	5	2
	b)	Draw basic model of FTP and its function in communication.	8M	5	4
		OR			
10.	a)	Explain broadcast, point to point and Multipoint networks.	7M	5	2
	b)	Classify Cryptography with their applications.	7M	5	4

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Hall Ticket Number :										

R-15

Code: 5G374

IV B.Tech. I Semester Supplementary Examinations July 2021

Digital Design Through Verilog HDL

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Explain in detail the different levels of design abstraction in Verilog. 8M

   b) How integers and real numbers can be declared in Verilog. 6M

OR

2. a) Differentiate between keywords & identifiers with suitable examples. 7M

   b) What are the different value set supported by Verilog. 7M

UNIT–II

3. a) Write a gate level verilog code for full adder using 2 half adders. 6M

   b) Write a verilog code and test bench for clocked RS flip-flop with NAND gates. 8M

OR

4. a) Write a verilog switch level description of CMOS inverter. 7M

   b) How propagation delays can be specified for switch primitives. 7M

UNIT–III

5. a) Illustrate with an example how delays can be combined with continuous assignments. 7M

   b) Write a verilog dataflow model for 4:1mux. 7M

OR

6. a) What are the features of initial construct in verilog. 6M

   b) Explain i)always construct ii)blocking vs non-blocking assignments 8M

UNIT–IV

7. a) Differentiate between functions and tasks. 6M

   b) Write a verilog module for parity generation through a function. 8M

OR

8. a) What are parameters? Design a half adder module with timing delays assigned through parameters. 7M

   b) What is an FSM? Differentiate between Mealy & Moore FSM. 7M

UNIT–V

9. a) What is SM chart? Explain how state graph can be converted to SM chart. 6M

   b) Derive SM chart for binary multiplier. 8M

OR

10. a) Tabulate different families of CPLD & FPGA. 7M

    b) What is one-hot assignment? Explain with an example. 7M

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Hall Ticket Number :										

R-15

Code: 5G375

IV B.Tech. I Semester Supplementary Examinations July 2021

Nano Electronics

(Electronics and Communication Engineering)

Max. Marks: 70 Time: 3 Hours

Answer *all five* units by choosing one question from each unit (5 x 14 = 70 Marks)

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UNIT–I

1. a) Discuss the process of Electron Microscopies? Explain the operation of Scanning probe Microscopies? 7M

   b) Explain the working principle of optical microscopy with neat sketches? 7M

OR

2. a) Define carbon nanotube? What are the types of carbon nano tubes, highlight the properties of carbon nano tubes? 7M

   b) List the methods for producing carbon nano tubes and explain any one of the method with a neat sketch? 7M

UNIT–II

3. a) Explain nano imprint lithography with a neat sketch? 7M

   b) Discuss about zero dimensional nano structures and write about quantum conductance of zero dimensional nano structures? 7M

OR

4. Brief out split-gate technology and also explain the process of self-assembly? 14M

UNIT–III

5. Explain Short channel MOS Transistor and split-gate transistor technologies? 14M

OR

6. a) Discuss quantum cellular automate with neat diagrams? 7M

   b) Describe the functioning of quantum dot array with proper sketches? 7M

UNIT–IV

7. a) What is RTDs? And explain three terminal RTDs technology? 7M

   b) Draw and explain digital circuit design based on RTDs technology of RTD 7M

OR

8. a) Explain the principle of SET and SET circuit design? 7M

   b) Comparison between FET and SET circuit design? 7M

UNIT–V

9. a) Explain the process of Energy supply and heat dissipation? 7M

   b) Discuss Limits due to thermal particle motion? 7M

OR

10. a) Write and explain Nano systems as information processing machines? 7M

    b) Explain the hardware requirements of nano systems? 7M

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