Hall Ticket Number :																
							R-15									
Code: 5G472 IV B.Tech. I Semester Supplementary Examinations July 2021																
Computer Networks																
(Electronics and Communication Engineering )																
Max. Marks: 70 Answer all five units by choosing one question from each unit ( 5 x 14 = 70 Marks ) ********																
														Marks	СО	Blooms Level
						UNIT	-1	]								Level
1.	a)	Illustrate each la	ayer i	in OS				]						7M	1	3
	b) Describe function of each layer in TCP/IP Model.										7M	1	2			
OR																
2.	a)	Demonstrate PS	STN	struct	ture v	with e	explai	natio	n.					8M	1	3
	b)	Discuss role of	•	otoco	ols 8	& the	eir s	tand	ards	refe	rred	in d	lata			
		communication.						1						6M	1	2
0	-)	Demonstrate	م برا دارم			UNIT			.					714	0	0
3.	a) b)	Demonstrate we		-		g win	aow l	oroto	COIS.					7M	2	3
b) Describe CSMA/CD in detail. 7M 2													2			
4.	a)	Summarize Mul	tinla	۵۰۵۹	ee Pi	<b>OF</b>								7M	2	2
4.	a) b)	Explain various	-					ate						7M	2	2
	5)			- 002										7 101	2	2
5.	a)	Compare adapt	ive a	nd no		-		Iting	algor	ithms	5.			8M	3	5
	b)	Give Outline of				•		•	•			addre	ess.	6M	3	4
						OF	ł									
6.	a)	Define fragment	tatior	and	expla	ain w	hy the	e IP4	and	IP6 p	rotoc	ols n	eed			
		to fragment some packets.										7M	3	1		
	b)	Examine role of	Con	gesti	on C	ontro	l Algo	orithr	ns in	com	munio	catior	٦.	7M	3	3
_	,				L	JNIT-										
7.	a)	Show TCP and						h de	script	ion.				8M	4	3
	b)	Draw the segme	ent si	ructu	ire of	OF								6M	4	4
8.	2)	Justify the perfo	rmar	nco is	20100			ort la	vorn	rotoc	ole			7M	4	5
0.	a) b)	Discuss applica					•		••••			n		7M	4	2
	5)								COM	mun	icatio			7 101	т	2
9.	a)	State advantage	es an	d lim	L			ic an	d sec	ret ke	ev en	crypt	ion.	6M	5	2
	b)	Draw basic mod					•				•			8M	5	4
	,					OF										
10.	a)	Explain broadca	ast, p	oint t	o poi	nt an	id Mu	Iltipoi	int ne	tworl	۲S.			7M	5	2
	b)	Classify Cryptog	graph	ny wit	h the	ir ap	plicat	ions.						7M	5	4
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Code: 5G374       R-15         R-15         Digital Design Through Verilog HDL (Electronics and Communication Engineering)         Max. Marks: 70       Time: 3 Hours         Answer all five units by choosing one question from each unit (5x14=70 Marks)       Ime: 3 Hours         UNIT-1       1. a)       Explain in detail the different levels of design abstraction in Verilog.       6M         b)       How integers and real numbers can be declared in Verilog.       6M         c)       OR       7M         2. a)       Differentiate between keywords & identifiers with suitable examples.       7M         b)       What are the different value set supported by Verilog.       7M         b)       Write a gate level verilog code for full adder using 2 half adders.       6M         b)       Write a verilog switch level description of CMOS inverter.       7M         b)       Write a verilog switch level description of CMOS inverter.       7M         b)       Write a verilog dataflow model for 4:1mux.       7M         c)       OR       6         c)       Write a verilog dataflow model for 4:1mux.       7M         b)       Write a verilog module for parity generation through a function.       8M         c)       OR       6       6         a	Hall	Tick	et Number :												
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Nano Electronics																	
(Electronics and Communication Engineering)												irc					
Max. Marks: 70 Answer all five units by choosing one question from each unit ( 5 x 14 = 70 Marks ) *********												12					
	UNIT–I																
1.	a)	Discuss the process of Electron Microscopies? Explain the operation of Scanning probe Microscopies? 71												7M			
	b)	Explain the working principle of optical microscopy with neat sketches? 7N												7M			
		OR															
2.	<ol> <li>a) Define carbon nanotube? What are the types of carbon nano tubes, highlight the properties of carbon nano tubes?</li> </ol>											the	7M				
	b)	List the methods for producing carbon nano tubes and explain any one of the method with a neat sketch? 7												7M			
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3.	a)	Explain nanc	o impr	int lit	hoar	aphv	with				•						7M
01	b)												um				
	~)	conductance							uctur						I		7M
4.		Brief out split	t-gate	e tech	nnolo	gy ar	nd als	so ex	plain	the p	oroce	ss of	self-a	assen	nbly?		14M
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5.		Explain Shor	t cha	nnel	MOS	5 Trai	nsisto	or and	d spli	t-gate	e trar	sisto	r tech	nolo	gies?		14M
								OF	R								
6.	a)	Discuss quar	ntum	cellu	lar a	utom	ate w	vith n	eat d	iagra	ms?						7M
	b)	Describe the	funct	tionir	ng of	quan	itum (	dot a	rray v	vith p	orope	r ske	tches	?			7M
							[	UN	IIT-I	V							
7.	a)	What is RTD			•							0.					7M
	b)	) Draw and explain digital circuit design based on RTDs technology of RTD												7M			
								OF									
8.	a)	Explain the p								-	)						7M
	b)	Comparison	ET and SET circuit design?											7M			
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9.	a)	Explain the p	roces	ss of	Enei	gy si	upply				patio	n?					7M
	b)	Discuss Limi				••					-						7M
	-							OF	ł								
10.	a)	Write and ex	-		-					-		ng ma	achine	es?			7M
	b)	Explain the h	ardw	are r	equii	eme	nts of		o sys	tems	;?						7M
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